■ BCM5201/BCM5202

10/100BASE-TX/FX Mini-Φ™ Transceiver

GENERAL DESCRIPTION

The BCM5201/5202 is a single-chip 10/100BASE-TX/FX transceiver targeted at Fast Ethernet switches and CardBus Network Interface devices. The BCM5201 operates at 3.3 volts while the BCM5202 operates at 5 volts. These devices contain a full-duplex 10BASE-T/100BASE-TX/100BASE-FX Fast Ethernet transceiver which performs all of the physical layer interface functions for 10BASE-T Ethernet on CAT 3, 4, and 5 unshielded twisted pair (UTP) cable and 100BASE-TX Fast Ethernet on CAT 5 UTP cable. 100BASE-FX is supported through the use of external fiber-optic transmit and receive devices.

The BCM5201/5202 is a highly integrated solution combining a digital adaptive equalizer, ADC, phase lock loop, line driver, encoder, decoder and all the required support circuitry into a single monolithic CMOS chip. It complies fully with the IEEE 802.3u specification, including the Media Independent Interface (MII) and Auto-Negotiation subsections, providing compatibility with all industry standard Fast Ethernet Media Access Controller (MAC) and repeater devices.

The effective use of digital technology in the BCM5201/5202 design results in robust performance over a broad range of operating scenarios. Problems inherent to mixed-signal implementations, such as analog offset and on-chip noise, are eliminated by employing field proven digital adaptive equalization and digital clock recovery techniques.

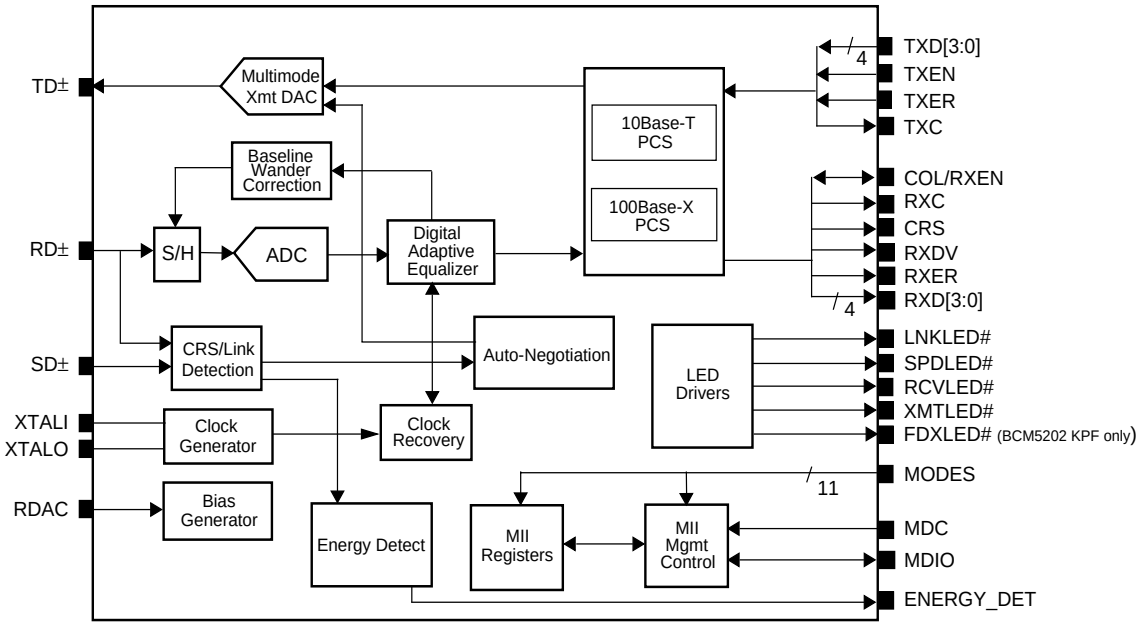
FEATURES

- 10BASE-T/100BASE-TX/FX IEEE 802.3u compliant
- Single-chip physical interface - MII to Magnetics
- 3.3 Volt (BCM5201) or 5 Volt (BCM5202) Operation
- Intelligent Power Management with cable signal detect
- Media Independent Interface (MII)
- Fully-integrated digital adaptive equalizer
- 125 MHz clock generator and timing recovery
- On-chip multi-mode transmit waveshaping
- Integrated digital baseline wander correction
- Full-duplex support
- IEEE 802.3u-compliant Auto-Negotiation
- MII management interface up to 12.5 Mbps
- LED status pins
- Loopback mode for diagnostics
- Internal Oscillator utilizes 25 MHz Crystal
- High Speed Token Ring frame length support
- Compatible with 3.3 Volt and 5 Volt I/O
- 64-Pin TQFP for low-profile applications
- 80-Pin MQFP for standard applications

APPLICATIONS

- PCMCIA and CardBus Adapter Cards
- PCI Rev 2.2 Adapter Cards
- Dual-Speed Switches
- Printers and Print Servers
- Transceiver Pods (MII MAU)
- Computer Motherboards
- Dual Speed Repeaters
- Token Ring adapters, switches, and hubs

Figure 1: Functional Block Diagram



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REVISION HISTORY

REVISION #	*DATE*	*CHANGE DESCRIPTION*
SP2.0	September 3, 1998	Preliminary Release
SP3.0	March 2, 1999	Final Release: 1. Page 12 10Base-T Serial Mode now includes details of associated signals (Table 4 was added). 2. Force100/10 Indication explanation updated on page 28 and 31. 3. Table 32, 100Base-X Receive Timings updated. 4. Table 41, Recommended operating conditions updated. 5. Table 43, Electrical characteristics updated. 6. Changed from “Preliminary” to “Final” (the qualifier “Preliminary” is removed).

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SECTION 1: FUNCTIONAL DESCRIPTION

OVERVIEW

The BCM5201/5202 is a single-chip Fast Ethernet transceiver. It performs all of the physical layer interface functions for 100BASE-TX full- or half-duplex Ethernet on CAT 5 twisted pair cable and 10BASE-T full- or half-duplex Ethernet on CAT 3, 4 or 5 cable. It may also be configured for 100BASE-FX full- or half-duplex transmission over fiber-optic cabling when paired with an external fiber-optic line driver and receiver.

The chip performs 4B5B, MLT3, NRZI, and Manchester encoding and decoding, clock and data recovery, stream cipher scrambling/descrambling, digital adaptive equalization, line transmission, carrier sense and link integrity monitor, Auto-Negotiation and Media Independent Interface (MII) management functions. The BCM5201/5202 may be connected to a MAC, switch controller or repeater controller through the MII on one side, and connects directly to the network media on the other side (through isolation transformers for unshielded twisted pair (UTP) modes or fiber-optic transmitter/receiver components for FX modes). In repeater mode, the MII port may be bussed with other BCM5201/5202 devices. The BCM5201/5202 is fully compliant with the IEEE 802.3 and 802.3u standards.

ENCODER/DECODER

In 100BASE-TX and 100BASE-FX modes, the BCM5201/5202 transmits and receives a continuous data stream on twisted pair or fiber-optic cable. When the MII transmit enable is asserted, nibble-wide (4-bit) data from the transmit data pins is encoded into 5-bit code-groups and inserted into the transmit data stream. The 4B5B encoding is shown in Table 1. The transmit packet is encapsulated by replacing the first two nibbles of preamble with a start of stream delimiter (J/K codes) and appending an end of stream delimiter (T/R codes) to the end of the packet. When the MII transmit error input is asserted during a packet, the transmit error code group (H) is sent in place of the corresponding data code group. The transmitter will repeatedly send the idle code group between packets.

In TX mode, the encoded data stream is scrambled by a stream cipher block and then serialized and encoded into MLT3 signal levels. A multi-mode transmit DAC is used to drive the MLT3 data onto the twisted pair cable. In FX mode, the scrambling function is bypassed and the data is NRZI encoded. The multimode transmit DAC drives differential positive ECL (PECL) levels to an external fiber-optic transmitter.

Following baseline wander correction, adaptive equalization, and clock recovery in TX mode, the receive data stream is converted from MLT3 to serial NRZ data. The NRZ data is descrambled by the stream cipher block and then deserialized and aligned into 5-bit code groups.

In FX mode, the receive data stream differential PECL levels are sampled from the fiber-optic receiver. Baseline wander correction, adaptive equalization, and stream cipher descrambling functions are bypassed and NRZI decoding is used instead of MLT3.

The 5-bit code groups are decoded into 4-bit data nibbles, as shown in Table 1. The start of stream delimiter is replaced with preamble nibbles and the end of stream delimiter and idle codes are replaced with all zeros. The decoded data is driven onto the MII receive data pins. When an invalid code group is detected in the data stream, the BCM5201/5202 will assert the MII RXER signal. The chip will also assert RXER for several other error conditions which improperly terminate the data stream. While RXER is asserted, the receive data pins will be driven with a 4-bit code indicating the type of error detected. The error codes are listed in Table 2.

In 10BASE-T mode, Manchester encoding and decoding is performed on the data stream. The multimode transmit DAC performs pre-equalization for 100 meters of CAT 3 cable.

LINK MONITOR

In 100BASE-TX mode, receive signal energy is detected by monitoring the receive pair for transitions in the signal level. Signal levels are qualified using squelch detect circuits. When no signal or certain invalid signals are detected on the receive pair, the link monitor will enter and remain in the “Link Fail” state where only idle codes will be transmitted. When a valid signal is detected on the receive pair for a minimum period of time, the link monitor will enter the “Link Pass” state and the transmit and receive functions will be enabled.

In 100BASE-FX mode, the external fiber-optic receiver performs the signal energy detection function and communicates this information directly to the BCM5201/5202 through the differential SD± pins.

In 10BASE-T mode, a link-pulse detection circuit constantly monitors the RD± pins for the presence of valid link pulses.

CARRIER SENSE

In 100BASE-X modes, carrier sense is asserted asynchronously on the CRS pin as soon as activity is detected in the receive data stream. RXDV is asserted as soon as a valid Start-of-Stream Delimiter (SSD) is detected. Carrier sense and RXDV are deasserted synchronously upon detection of a valid end of stream delimiter or two consecutive idle code groups in the receive data stream. If carrier sense is asserted and a valid SSD is not detected immediately, then RXER will be asserted in place of RXDV. A value of “1110” will be driven on the receive data pins to indicate false carrier sense.

In 10BASE-T mode, carrier sense is asserted asynchronously on the CRS pin when valid preamble activity is detected on the RD+/– input pins.

In half-duplex DTE mode, the BCM5201/5202 will also assert carrier sense while transmit enable is asserted and the link monitor is in the “Pass” state. In full-duplex mode, CRS is only asserted for receive activity.

COLLISION DETECTION

In half-duplex mode, collision detect is asserted on the COL pin whenever carrier sense is asserted and transmission is in progress. Collision detect is never asserted in full-duplex mode or repeater mode.

AUTO-NEGOTIATION

The BCM5201/5202 contains the ability to negotiate its mode of operation over the twisted pair link using the Auto-Negotiation mechanism defined in the IEEE 802.3u specification. Auto-Negotiation may be enabled or disabled by hardware or software control. When the Auto-Negotiation function is enabled, the BCM5201/5202 will automatically choose its mode of operation by advertising its abilities and comparing them with those received from its link partner. The BCM5201/5202 can be configured to advertise 100BASE-TX full-duplex and/or half-duplex and 10BASE-T full and/or half-duplex. The transceiver will negotiate with its link partner, and choose the highest level of operation available for its own link. Auto-Negotiation is not operational during 100BASE-FX operation and will not advertise full-duplex abilities when the device is configured in repeater mode.

DIGITAL ADAPTIVE EQUALIZER

The digital adaptive equalizer removes Intersymbol Interference (ISI) created by the transmission channel media. The equalizer accepts sampled unequalized data from the ADC on each channel and produces equalized data. The BCM5201/5202 achieves an optimum signal to noise ratio by using a combination of feed forward equalization and decision feedback equalization. This powerful technique achieves a 100BASE-TX BER of less than 1×10^{-12} for transmission up to 100 meters on CAT 5 twisted pair cable, even in harsh noise environments. The digital adaptive equalizers in the BCM5201/5202 achieve performance close to theoretical limits. The all-digital nature of the design makes the performance very tolerant to on-chip noise. The filter coefficients are self adapting to any quality of cable or cable length. Due to transmit pre-equalization in 10BASE-T mode and complete lack of ISI in 100BASE-FX mode, the adaptive equalizer is bypassed in these two modes of operation.

ADC

The receive channel has a 6-bit 125 MHz analog to digital converter (ADC). The ADC samples the incoming data on the receive channel and produces a 6-bit output. The output of the ADC is fed to the digital adaptive equalizer. Advanced analog circuit techniques achieve low offset, high power supply noise rejection, fast settling time, and low bit error rate.

DIGITAL CLOCK RECOVERY/GENERATOR

The all-digital clock recovery and generator block creates all internal transmit and receive clocks. The transmit clock is locked to the 25 MHz clock input while the receive clock is locked to the incoming data stream. Clock recovery circuits optimized to MLT3, NRZI, and Manchester encoding schemes are included for use with each of the three different operating modes. The input data stream is sampled by the recovered clock and fed synchronously to the digital adaptive equalizer.

BASELINE WANDER CORRECTION

A 100BASE-TX data stream is not always DC balanced. Because the receive signal must pass through a transformer, the DC offset of the differential receive input can wander. This effect, known as baseline wander, can greatly reduce the noise immunity of the receiver. The BCM5201/5202 automatically compensates for baseline wander by removing the DC offset from the input signal, and thereby significantly reduces the chance of a receive symbol error. The baseline wander correction circuit is not required, and therefore bypassed, in 10BASE-T and 100BASE-FX operating modes.

MULTIMODE TRANSMIT DAC

The multimode transmit digital to analog converter (DAC) transmits MLT3-coded symbols in 100BASE-TX mode, NRZI-coded symbols in 100BASE-FX mode, and Manchester-coded symbols in 10BASE-T mode. It allows programmable edge-rate control in TX mode which decreases unwanted high frequency signal components thus reducing EMI. High-frequency pre-emphasis is performed in 10BASE-T mode; no filtering is performed in 100BASE-FX mode. The transmit DAC utilizes a current drive output which is well balanced and produces very low-noise transmit signals. PECL voltage levels are produced with resistive terminations in 100BASE-FX mode.

STREAM CIPHER

In 100BASE-TX mode, the transmit data stream is scrambled in order to reduce radiated emissions on the twisted pair cable. The data is scrambled by *exclusive or'ing* the NRZ signal with the output of an 11-bit wide linear feedback shift register (LFSR), which produces a 2047-bit non-repeating sequence. The scrambler reduces peak emissions by randomly spreading the signal energy over the transmit frequency range, and eliminating peaks at certain frequencies.

The receiver descrambles the incoming data stream by *exclusive or'ing* it with the same sequence generated at the transmitter. The descrambler detects the state of the transmit LFSR by looking for a sequence representing consecutive idle codes. The descrambler will "lock" to the scrambler state after detecting a sufficient number of consecutive idle code-groups. The receiver will not attempt to decode the data stream unless the descrambler is locked. Once locked, the descrambler will continuously monitor the data stream to make sure that it has not lost synchronization. The receive data stream is expected to contain inter-packet idle periods. If the descrambler does not detect enough idle codes within 724µs, it will become "unlocked," and the receive decoder will be disabled. The descrambler will always be forced into the "unlocked" state when a link failure condition is detected.

A special node called High Speed Token Ring can be enabled. It will increase the scrambler timeout from 724 µs to 5816 µs, thus allowing frames as large as the Token Ring maximum length to be received without error.

Stream cipher scrambling/descrambling is not used in 100BASE-FX and 10BASE-T modes.

FAR-END FAULT

Auto-Negotiation provides a Remote Fault capability for detection of asymmetric link failures. Since Auto-Negotiation is not available for 100BASE-FX, the BCM5201/5202 implements the IEEE 802.3 standard Far-End Fault mechanism for the indication and detection of remote error conditions. When the Far-End Fault mechanism is enabled, a transceiver will transmit the Far-End Fault Indication whenever a receive channel failure is detected (signal detect is deasserted). The transceiver will also continuously monitor the receive channel when a valid signal is present (signal detect asserted). When its link partner is indicating a remote error, the transceiver will force its link monitor into the link fail state and set the Remote Fault bit in the MII status register. The Far-End Fault mechanism is enabled by default in 100BASE-FX mode and disabled in 100BASE-TX and 10BASE-T modes, and may be controlled by software after reset.

MII MANAGEMENT

The BCM5201/5202 contains a complete set of MII management registers accessible by using the management clock line (MDC) and the bidirectional serial data line (MDIO). Many transceivers can be bussed together on a single MDIO/MDC wire pair by giving each a unique PHY address, defined by configuring the five external PHY address input pins.

Every time an MII read or write operation is executed, the BCM5201/5202 compares the operation's PHY address with its own PHY address definition. The operation is executed only when the addresses match.

For further details, see Section 5: Register Summary on page 15.

Table 1: 4B5B Encoding

NAME	*4B CODE*	*5B CODE*	*MEANING*
0	0000	11110	Data 0
1	0001	01001	Data 1
2	0010	10100	Data 2
3	0011	10101	Data 3
4	0100	01010	Data 4
5	0101	01011	Data 5
6	0110	01110	Data 6
7	0111	01111	Data 7
8	1000	10010	Data 8
9	1001	10011	Data 9
A	1010	10110	Data A
B	1011	10111	Data B
C	1100	11010	Data C
D	1101	11011	Data D
E	1110	11100	Data E
F	1111	11101	Data F
I	0000*	11111	Idle
J	0101*	11000	Start-of-Stream Delimiter, Part 1
K	0101*	10001	Start-of-Stream Delimiter, Part 2
T	0000*	01101	End-of-Stream Delimiter, Part 1
R	0000*	00111	End-of-Stream Delimiter, Part 2
H	1000	00100	Transmit Error (used to force signalling errors)
V	0111	00000	Invalid Code
V	0111	00001	Invalid Code
V	0111	00010	Invalid Code
V	0111	00011	Invalid Code
V	0111	00101	Invalid Code
V	0111	00110	Invalid Code
V	0111	01000	Invalid Code
V	0111	011000	Invalid Code
V	0111	10000	Invalid Code
V	0111	11001	Invalid Code
* Treated as invalid code (mapped to 0111) when received in data field.			

Table 2: Receive Error Encoding

ERROR TYPE	*RXD[3:0]*
Stream cipher error - descrambler lost lock	0010
Link failure	0011
Premature end of stream	0110
Invalid code	0111
Transmit error	1000
False carrier sense	1110

SECTION 2: HARDWARE SIGNAL DEFINITION TABLE

Table 3 provides the pin descriptions for the BCM5201 and BCM5202.

Table 3: Pin Descriptions

5201 KPT	*5202 KET*	*5202 KPF*	*PIN LABEL*	*TYPE*	*DESCRIPTION*
MEDIA CONNECTIONS					
26, 25	26, 25	31, 30	RD+ RD–	I	**Receive Pair.** Differential data from the media is received on the RD± signal pair.
31, 30	31, 30	36, 35	TD+ TD–	O	**Transmit Pair.** Differential data is transmitted to the media on the TD± signal pair.
CLOCK					
6, 5	6, 5	8, 7	XTALI, XTALO	I,O	**25 MHz Crystal Oscillator Input, Output.** A 25 MHz parallel-resonant crystal may be connected between these pins to stabilize the internal oscillator. Connect a 27 pF capacitor from each pin to GND. Alternatively, a stable 25 MHz clock may be applied to the XTALI pin. In this case, leave XTALO unconnected. No capacitors are required.
MII INTERFACE					
53	53	67	TXC	O	**Transmit Clock.** 25 MHz output in 100BASE-X mode and 2.5 MHz in 10BASE-T MII mode. 10 MHz output in 10BASE-T serial mode. This clock is a continuously driven output, generated from the XTALI input.
60, 59, 58, 57	60, 59, 58, 57	74, 73, 72, 71	TXD[3:0]	I_{PD}	**Transmit Data Input.** Nibble-wide transmit data stream is input on these pins synchronous with TXC. TXD[3] is the most significant bit. Only bit 0 is used in 10BASE-T serial mode.
56	56	70	TXEN	I_{PD}	**Transmit Enable.** Active high. Indicates that the data nibble on TXD[3:0] is valid.
52	52	66	TXER	I_{PD}	**Transmit Error.** An active high input is asserted when a transmit error condition is requested by the repeater controller.
50	50	64	RXC	O	**Receive Clock.** 25 MHz output in 100BASE-X MII mode and 2.5 MHz output in 10BASE-T mode. 10 MHz output in 10BASE-T serial mode. This clock is recovered from the incoming data on the cable inputs. RXC is a continuously running output clock resynchronized at the start of each incoming packet. This synchronization may result in an elongated period during one cycle while RXDV is low.
43, 44, 47, 48	43, 44, 47, 48	53, 54, 57, 58	RXD[3:0]	O	**Receive Data Outputs.** Nibble-wide receive data stream is driven out on these pins synchronous with RXC. RXD[3] is the most significant bit. Only bit 0 is used in 10BASE-T serial mode.
49	49	63	RXDV	O	**Receive Data Valid.** Active high. Indicates that a receive frame is in progress, and that the data stream present on the RXD output pins is valid.
51	51	65	RXER	O	**Receive Error Detected.** Active high. Indicates that an error is occurring during a receive frame.

[MSB:LSB]; # = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Table 3: Pin Descriptions (Continued)

5201 KPT	*5202 KET*	*5202 KPF*	*PIN LABEL*	*TYPE*	*DESCRIPTION*
62	62	76	CRS	O	**Carrier Sense.** Active high. Indicates traffic on link. In 100BASE-X modes, CRS is asserted when a non-idle condition is detected in the receive data stream and deasserted when idle or a valid end of stream delimiter is detected. In 10BASE-T mode, CRS is asserted when a valid preamble is detected and deasserted when end-of-file or an idle condition is detected. CRS is also asserted during transmission of packets except in repeater or full-duplex modes. CRS is an asynchronous output signal.
61	61	75	COL/RXEN	I/O_{PD}	**Collision Detect.** In half-duplex modes, active high output indicates that a collision has occurred. In full-duplex mode, COL remains low. COL is an asynchronous output signal. **Receive Enable.** In repeater mode, RXEN becomes an active high input allowing the repeater controller to enable the MII receive bus.
41	41	51	MDIO	I/O_{PU}	**Management Data I/O.** This serial input/output bit is used to read from and write to the MII registers. The data value on the MDIO pin is valid and latched on the rising edge of MDC.
42	42	52	MDC	I_{PD}	**Management Data Clock.** The MDC clock input must be provided to allow MII management functions. Clock frequencies up to 12.5 MHz are supported.
9	9	11	RESET#	I_{PU}	**Reset.** Active Low. Resets the BCM5201/5202. Also used to enable Power Off and Low Power modes.
MODE					
14, 13, 12, 11, 10	14, 13, 12, 11, 10	16, 15, 14, 13, 12	PHYAD [4:0]	I_{PD}	**PHY Address Selects.** These inputs set the MII management PHY address.
39	39	49	FDX	I_{PD}	**Full-Duplex Mode.** When Auto-Negotiation is disabled, the FDX pin is logically OR'ed with register 00, bit 8 to select full-duplex (1) or half-duplex (0) operation. This selection is only performed in DTE mode as full-duplex operation is not allowed in repeater mode.
37	37	47	F100/SD+	I	**100BASE-FX Signal Detect/Force 100BASE-X Control.** When 100BASE-FX is selected, SD+ and SD– indicate signal quality status on the fiber optic link. When the signal quality is good, the SD+ pin will be high relative to the SD– pin. When 100BASE-FX mode is not selected, the F100 function is enabled. When F100 is high and ANEN is low, the transceiver will be forced to 100BASE-TX operation. When F100 is low and ANEN is low, the transceiver is forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation.
38	38	48	ANEN/SD–	I	**100BASE-FX Signal Detect/Auto-Negotiation Enable.** When 100BASE-FX is selected, the SD– function is enabled. See SD+ description above. When 100BASE-FX is not selected, the ANEN function is enabled. ANEN is active high. When pulled high, Auto-Negotiation will begin immediately after reset. When low, Auto-Negotiation is disabled by default. After reset, the Auto-Negotiation function is under software control.
15	15	17	TESTEN	I_{PD}	**Test Mode Enable.** Active high. May float or be grounded for normal operation.

[MSB:LSB]; # = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

Table 3: Pin Descriptions (Continued)

5201 KPT	*5202 KET*	*5202 KPF*	*PIN LABEL*	*TYPE*	*DESCRIPTION*
16	16	18	LOWPWR	I_{PD}	**Low Power Mode Enable.** Active high input places the BCM5201/5202 into Low Power operation with the chip deactivated except for the energy detect block and the crystal oscillator. When asserted with RESET# pulled low, the entire chip is deactivated (Power Off mode).
17	17	19	ENERGY_DET	O	**Energy Detection.** Active high output indicates the presence of a signal on RD+/– receive analog wire pair. Operational in all modes except Power Off.
BIAS					
23	23	28	RDAC	B	**DAC Bias Resistor.** Adjusts the current level of the transmit DAC. A resistor of 1.27 kΩ ±1% must be connected between the RDAC pin and GND.
LEDS					
35	35	45	LNKLED#	I/O_{PU}	**Link Integrity LED.** The Link Integrity LED indicates the link status of the PHY. LNKLED# is driven low when the link to the PHY is good. During RESET, the output driver is tri-stated and the input value is used to latch the fiber mode. If the pin is low, 100BASE-FX mode is selected. If the pin is high or floating, 10BASE-T or 100BASE-TX mode is selected. When FX mode is enabled, the polarity of LINKLED# is inverted.
36	36	46	SPDLED#	I/O_{PU}	**100BASE-X LED.** The 100 Base-X LED is driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes. During RESET, the output driver is tri-stated and the input value is used to latch the repeater mode. If the pin is pulled low, the chip will enter repeater mode. If the pin is high or floating, DTE mode is selected. When repeater mode is enabled, the polarity of SPDLED# is inverted.
34	34	44	XMTLED# INTR# FDXLED#	O_{OD}	**Transmit Activity LED.** Active low output. The transmit activity LED is driven low for approximately 80ms each time there is transmit activity while in the link pass state. When the interrupt mode is enabled, pin becomes INTR#. When FDXLED mode is enabled, pin becomes FDXLED#.
33	33	43	RCVLED# ACTLED#	O_{OD}	**Receive Activity LED.** Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. In either interrupt or FDXLED mode, pin becomes ACTLED#, indicating both receive and transmit activity.
		20	FDXLED#	O	**Full Duplex LED.** BCM5202KPF 80-Pin Package Only. The Full Duplex LED is driven low when operating in full duplex mode and driven high in half duplex mode. This output always relates the duplex status, regardless of what type of output appears on the XMTLED# pin.
POWER					
8			IVDD	PWR	**Input VDD, BCM5201.** 3.3V or 5V. If any of the inputs are driven to 5.0V, this pin must be connected to a 5.0V supply. If none of the inputs are driven above 3.3V, this pin must be connected to the 3.3V supply.
	8	10	IVDD	PWR	**Input VDD, BCM5202.** This pin must be connected to the 5.0V supply.
[MSB:LSB]; # = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground					

Table 3: Pin Descriptions (Continued)

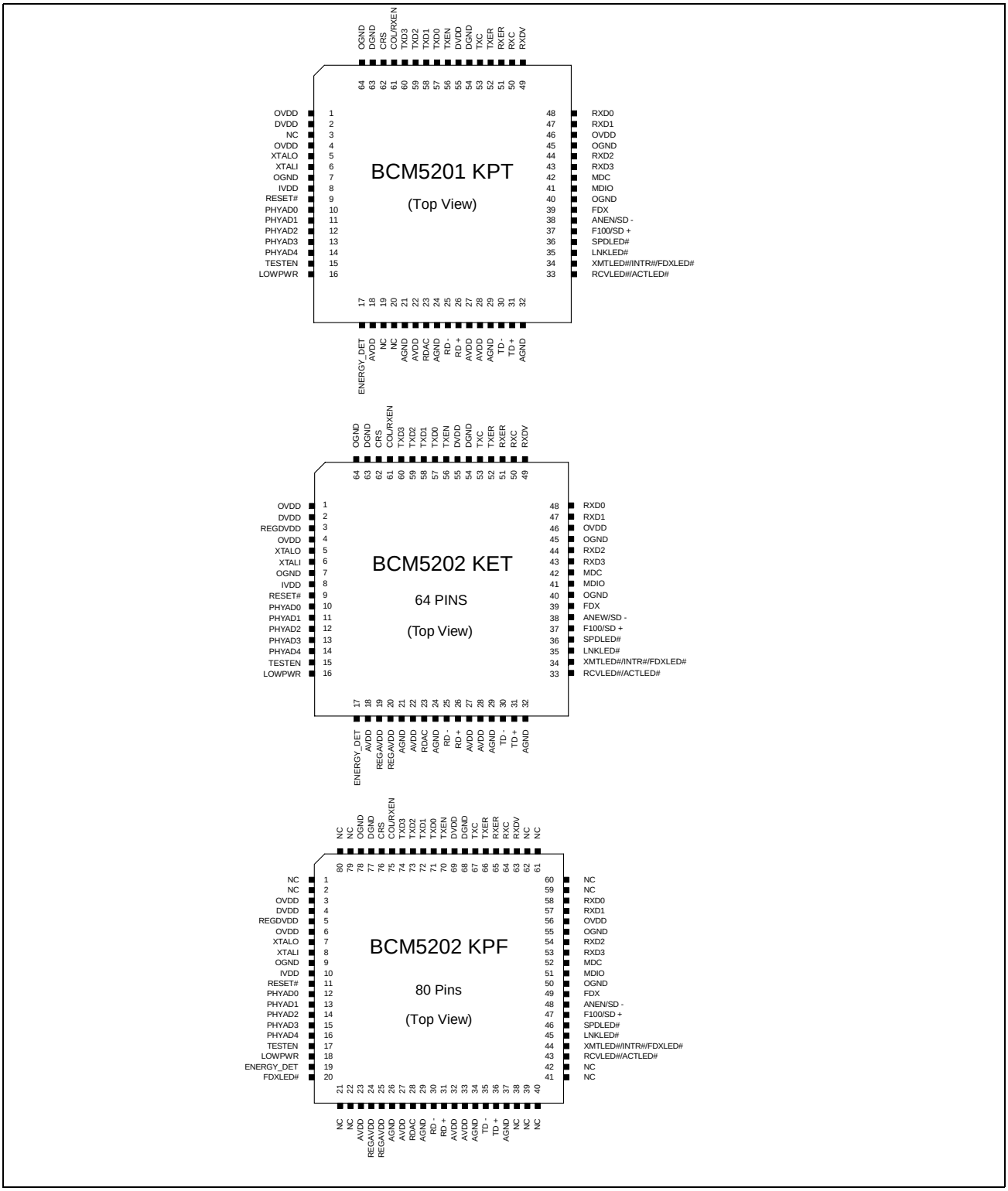
5201 KPT	*5202 KET*	*5202 KPF*	*PIN LABEL*	*TYPE*	*DESCRIPTION*
18, 22, 27, 28	18, 22, 27, 28	23, 27, 32, 33	AVDD	PWR	**Analog VDD.**
21, 24, 29, 32	21, 24, 29, 32	26, 29, 34, 37	AGND	GND	**Analog GND.**
	3	5	REGDVDD	PWR	**Voltage Regulator Input.** BCM5202 Only.
	19, 20	24, 25	REGAVDD	PWR	**Voltage Regulator Input.** BCM5202 Only.
2, 55	2, 55	4, 69	DVDD	PWR	**Digital Core VDD.**
54, 63	54, 63	68, 77	DGND	GND	**Digital Core GND.**
1, 4, 46	1, 4, 46	3, 6, 56	OVDD	PWR	**Digital Periphery (Output Buffer) VDD.**
7, 40, 45, 64	7, 40, 45, 64	9, 50, 55, 78	OGND	GND	**Digital Periphery (Output Buffer) GND.**

[MSB:LSB]; # = active-low signal, I = input, O = output, I/O = bidirectional, I_{PU} = input w/ internal pull-up, O_{OD} = open-drain output, O_{3S} = three-state output, B = Bias, PWR = power supply, GND = ground

SECTION 3: PINOUT DIAGRAMS

Figure 2 provides the pin diagrams for the BCM5201 and BCM5202.

Figure 2: Pin Diagrams



SECTION 4: OPERATIONAL DESCRIPTION

RESET

There are two ways to reset the BCM5201/5202. A hardware reset pin has been provided that resets all internal nodes in the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to the BCM5201/5202 after power-up.

The BCM5201/5202 also has a software reset capability. To perform software reset, a “1” must be written to bit 15 of the MII Control Register. This bit is self-clearing, meaning that a second write operation is not necessary to end the reset. There is no effect if a “0” is written to the MII Control Register reset bit.

MODE LATCHING

In order to reduce chip pin count, two pins have been given dual functionality. The LNKLED# and SPDLED# pins, normally LED drivers, are used as inputs during hardware RESET to sample requests for fiber mode and repeater mode operation. After RESET, the pins revert to outputs.

The LNKLED# pin will interpret a “0” during hardware RESET to be a request for fiber mode of operation and a “1” to be a request for copper UTP operation. Similarly, a “1” on the SPDLED# pin during hardware RESET will be interpreted as a request for DTE mode and a “0” a request for repeater mode.

The connection of the LED to the chip must be modified as shown in Figure 15, on page 45, to provide the signal input, yet retain the LED indication function. If it is desired to have either pin sample a “1” during RESET, the LED would be connected from the pin to VDD as in Figure 15A. To sample a “0” during RESET, the LED would be connected from the pin to ground as in Figure 15B. After the chip samples the input, it will latch the value and generate the proper polarity signal to drive the LED. For example, if either LED pin is sampled as “0” during RESET, the subsequent output signal becomes inverted, active high. This potential inversion of signal polarity may need to be accounted for if loads other than the LEDs are driven from these terminals.

If no connection is made to the LNKLED# or SPDLED# pins, internal pull-ups cause the chip to sample a logical “1” at reset and give the default operation of copper UTP mode and DTE.

CLOCK INPUT

The BCM5201/5202 clock input can be driven two ways: internal crystal oscillator or external oscillator. To take advantage of the internal oscillator, attach a 25 MHz crystal between the XTALI and XTALO pins. Connect 27 pF capacitors from each pin to ground. Alternatively, a 50% duty cycle 25MHz clock may be directly applied to the XTALI pin. In this case, the XTALO output must be left unconnected. No capacitors are used.

ISOLATE MODE

When the BCM5201/5202 is put into isolate mode, all MII inputs (TXD[3:0], TXEN, and TXER) are ignored, and all MII outputs (TXC, COL, CRS, RXC, RXDV, RXER, and RXD[3:0]) are set to high impedance. Only the MII management pins (MDC, MDIO) operate normally. Upon resetting the chip, the isolate mode is off. Writing a “1” to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a “0” to the same bit removes it from isolate mode.

LOOPBACK MODE

Loopback mode allows in-circuit testing of the BCM5201/5202 chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. The loopback mode is enabled by writing a “1” to bit 14 of the MII Control Register. In order to resume normal operation, bit 14 of the MII Control Register must be “0”.

Incoming packets on the cable are ignored in loopback mode. Because of this, the COL pin will normally not be activated during loopback mode. In order to test that the COL pin is actually working, the BCM5201/5202 may be placed into collision test mode. This mode is enabled by writing a “1” to bit 7 of the MII Control Register. Asserting TXEN will cause the COL output to go high, and deasserting TXEN will cause the COL output to go low.

While in loopback mode, several function bypass modes are also available that can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include: bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder. All bypass modes can be accessed by writing bits of the Auxiliary Control Register (10h).

Important Note: Due to the nature of the Block RXDV mode (bit 9 of MII Register 1Bh), which is enabled by default, 10BASE-T loopback will not function properly. It is necessary to first disable the Block RXDV mode by writing “FD00” to the Aux Mode 2 Register (1Bh).

FULL-DUPLEX MODE

The BCM5201/5202 supports full-duplex operation. While in full-duplex mode, a transceiver may simultaneously transmit and receive packets on the cable. The COL signal is never activated while in full-duplex mode. The CRS output is asserted only during receive packets, not transmit packets.

By default, the BCM5201/5202 powers up in half-duplex mode. When Auto-Negotiation is disabled, full-duplex operation can be enabled either by FDX pin control or by an MII register bit (Register 0, bit 8).

When Auto-Negotiation is enabled in DTE mode, full-duplex capability is advertised by default, but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h). In repeater mode, full-duplex capability can never be advertised.

One of the LED outputs can be modified to signal full-duplex vs. half-duplex operation. This capability is enabled by setting MII Register 1Ah, bit 15. In this mode, XMTLED# becomes FDXLED#, where a “1” output indicates half-duplex and a “0” output indicates full-duplex. This value is the inverse of MII register 18h, bit 0. When the FDXLED mode is activated, the RCVLED# becomes ACTLED#.

The BCM5202 KPF also contains a dedicated FDXLED# pin that is always active regardless of the type of output appearing on the XMTLED# pin.

REPEATER MODE

The BCM5201/5202 supports a repeater mode for 100Mbps operation only. Activation of this mode requires a pulldown resistor on the SPDLED# output. The pin is tri-stated during hardware reset and the value is sampled on the trailing edge of RESET#. While in the repeater mode, the BCM5201/5202 allows only 100BASE-TX or 100BASE-FX operation.

Several signals change their functionality in repeater mode. The COL output becomes a RXEN input, allowing the repeater controller to enable the MII receive bus. The CRS output is asserted only during receive packets, not transmit packets. No full-duplex operation is allowed.

100BASE-FX MODE

For 100BASE-FX mode, the BCM5201/5202 transceiver interfaces with an external 100BASE-FX fiber-optic driver and receiver instead of the magnetics module used with twisted-pair cable. The differential transmit and receive data pairs operate at PECL voltage levels instead of those required for twisted-pair transmission. The data stream is encoded using two-level NRZI instead of three-level MLT3. Since scrambling is not used in 100BASE-FX operation, the stream cipher function is bypassed.

To activate the 100BASE-FX mode, a pull down resistor must be placed on the LNKLED# output. During hardware reset, the output driver is tri-stated and the value is sampled on the trailing edge of RESET#.

The external fiber-optic receiver will detect signal status and pass it into the BCM5201/5202 through the SD± pins. The SD± pins are functional only after the 100BASE-FX mode is selected.

10BASE-T MODE

The same magnetics module used in 100BASE-TX mode can be used to interface to the twisted-pair cable when operating in 10BASE-T mode. The data will be two-level Manchester encoded instead of three-level MLT3 and no scrambling/ descrambling or 4B5B coding is performed. Data and clock rates are decreased by a factor of 10, with the MII interface signals operating at 2.5 MHz.

10BASE-T SERIAL MODE

The BCM5201/5202 supports 10BASE-T serial mode, also know as the 7-wire interface. In this mode, 10BASE-T transmit and receive packets appear at the MII in serial fashion, at a rate of 10 MHz. Receive packet data is output on RXD (0) synchronously with RXC. Transmit packet data must be input on TXD (0) synchronously with TXC. Both clocks toggle at 10 MHz.

The 10BASE-T serial mode is enabled by writing a “1” to bit 1 of the Auxiliary Multiple-PHY register (1Eh). Note that this mode is not available in 100BASE-X modes. The following table shows the MII pins used in this mode and their direction of operation.

Table 4: 10BASE-T Serial Mode (7-Wire) Signals

5201 KPT	*5202 KET*	*5202 KPF*	*PIN LABEL*	*TYPE*	*DESCRIPTION*
57	57	71	TXD (0)	I	Serial Transmit Data
53	53	67	TXC	O	Tranmit Data Clock (10 MHz)
56	56	70	TXEN	I	Transmit Enable
48	48	58	RXD (0)	O	Serial Receive Data
50	50	64	RXC	O	Receive Data Clock (10 MHz)
62	62	76	CRS	O	Carrier Sense
61	61	61	COL/RXEN	O	Collision Detect

SPECIAL LED MODES

Traffic Meter Mode. The blink rate of XMTLED# and RCVLED# is decreased dramatically to better show the volume of traffic. Lower traffic levels will make the corresponding LED appear dimmer than higher traffic levels. This mode is activated by writing a “1” to bit 6 of the Aux Mode 2 register (1Bh).

Two Link LED Mode. In this mode, the functions of SPDLED# and LNKLED# are changed. SPDLED# becomes an indicator of 10BASE-T link while LNKLED# becomes an indicator of 100BASE-X link. The Two Link LED mode is enabled by writing a “1” to bit 2 of the Aux Mode 2 Register (1Bh). Note that the polarities of these two outputs are influenced by whether FX mode or RPTR mode are enabled. See the definitions of SPDLED# and LNKLED# pins.

Force LEDs On. The XMTLED# and RCVLED# outputs can be forced on (“0” value) by writing a “1” to bit 5 of the Aux Mode 2 register(1Bh).

Disable LEDs. The XMTLED# and RCVLED# outputs can be forced off (“1” value) by writing a “1” to bit 4 of the Aux Mode register (1Dh). Similarly, the LNKLED# output can be forced off (value depends on FX mode, see definition of LNKLED# pin) by writing a “1” to bit 3 of the Aux Mode register (1Dh).

INTERRUPT MODE

The BCM5201/5202 can be programmed to provide an interrupt output. Three conditions can cause an interrupt to be generated: changes in the duplex mode, changes in the speed of operation or changes in the link status. The interrupt feature is disabled by default. When the interrupt capability is enabled by setting MII register 1Ah, bit 14, the XMTLED# pin becomes the INTR# pin and the RCVLED# pin becomes an “activity” pin named ACTLED#. The INTR# pin is open-drain and may be wire-ORed with INTR# pins of other chips on a board. The status of each interrupt source is reflected in register 1Ah, bits 1, 2 and 3. If any type of interrupt occurs, the Interrupt Status bit, register 1Ah, bit 0, will be set.

The Interrupt Register (1Ah) also contains several bits to control different facets of the interrupt function. If the interrupt enable bit is set to “0”, no status bits will be set and no interrupts will be generated. If the interrupt enable bit is set to “1”, the following conditions apply:

1. If mask status bits (bits 9,10,11) are set to “0” and the interrupt mask (bit 8) is set to “0”, status bits and interrupts will be available.
2. If mask status bits (bits 9,10,11) are set to “0” and the interrupt mask (bit 8) is set to “1”, status bits will be set but no interrupts generated.
3. If any mask status bit is set to “1” and the interrupt mask is set to “0”, that status bit will not be set and no interrupt of that type will be generated.
4. If any mask status bit is set to “1” and the interrupt mask is set to “1”, that status bit will not be set and no interrupt of any kind will be generated.

POWER SAVING MODES

Two power saving modes are implemented in the BCM5201/5202, which target PCMCIA and CardBus applications. The first, called Power Off, disables all circuitry on the chip and consumes the least amount of power. In this mode, register contents are not preserved. Thus, a hard reset should be issued at least 2 milliseconds after exiting this mode. The Power Off mode is enabled by setting LOWPWR to “1” and RESET# to “0”.

The second power saving mode is Low Power. In this modes, all chip circuitry is disabled except for the crystal oscillator and the special Energy Detection function. This mode is useful for determining whether the transceiver is connected to a link partner. The Energy Detection block outputs its result on the ENERGYDET pin which can be used by external logic to control when the transceiver is placed in Full Power or Low Power modes. Register contents are preserved while the chip is in Low Power mode, so a hard reset is not necessary after resuming Full Power. The Low Power Mode is enabled by setting LOWPWR to “1” and RESET# to “1”.

Table 5: Power Modes

MODE	*OSCILLATOR AND ENERGY DETECTION*	*LOWPWR*	*RESET#*
Full Power	Active	0	X
Low Power	Active	1	1
Power Off	Disabled	1	0

ENERGY DETECTION

An on-chip Energy Detection circuit has the capability of determining when a link partner is connected to the end of the transmission media. The circuit monitors the receive inputs for any type of energy, including 10BASE-T, 100BASE-TX or 100BASE-FX packets, and 10BASE-T or Auto-Negotiation link pulses. When energy is detected on the receive inputs for longer than 1.3 milliseconds, the ENERGYDET output is asserted. If all traces of energy disappear for longer the 1.3 seconds, it is assumed that the link partner has disconnected, and the ENERGYDET output is deasserted. The Energy Detection circuit is operational in both Full Power and Low Power modes.

In addition, there is a special mode called Automatic Low Power which is enabled by writing a “1” to bit 3 of the Aux Mode 2 register (1Bh). In this mode, a loss of energy on the receive inputs automatically causes the chip to enter the Low Power mode. Similarly, the next time energy is detected, the chip will resume Full Power mode.

SECTION 5: REGISTER SUMMARY

MEDIA INDEPENDENT INTERFACE (MII) MANAGEMENT INTERFACE: REGISTER PROGRAMMING

The BCM5201/5202 fully complies with the IEEE 802.3u Media Independent Interface (MII) specification. The MII management interface registers are serially written-to and read-from using the MDIO and MDC pins. A single clock waveform must be provided to the BCM5201/5202 at a rate of 0-12.5 MHz through the MDC pin. The serial data is communicated on the MDIO pin. Every MDIO bit must have the same period as the MDC clock. The MDIO bits are latched on the rising edge of the MDC clock.

See Table 6 for the fields in every MII instruction's read or write packet frame.

Table 6: MII Management Frame Format

OPERATION	*PRE*	*ST*	*OP*	*PHYAD*	*REGAD*	*TA*	*DATA*	*IDLE*	*DIRECTION*
READ	1 ... 1	01	10	AAAAA	RRRRR	ZZ Z0	Z ... Z D ... D	Z Z	Driven to BCM5201/5202 Driven by BCM5201/5202
WRITE	1 ... 1	01	01	AAAAA	RRRRR	10	D ... D	Z	Driven to BCM5201/5202

Preamble (PRE). Thirty two consecutive "1" bits must be sent through the MDIO pin to the BCM5201/5202 to signal the beginning of an MII instruction. Fewer than 32 "1" bits will cause the remainder of the instruction to be ignored, unless the Preamble Suppression mode is enabled (register 01, bit 6).

Start of Frame (ST). A "01" pattern indicates that the start of the instruction follows.

Operation Code (OP). A READ instruction is indicated by "10", while a WRITE instruction is indicated by "01".

PHY Address (PHYAD). A 5-bit PHY address follows next, with the MSB transmitted first. The PHY address allows a single MDIO bus to access multiple transceivers. The BCM5201/5202 supports the full 32-PHY address space.

Register Address (REGAD). A 5-bit Register Address follows, with the MSB transmitted first. The register map of the BCM5201/5202, containing register addresses and bit definitions, are provided on the following pages.

Turnaround (TA). The next two bit times are used to avoid contention on the MDIO pin when a Read operation is performed. For a Write operation, "10" must be sent to the chip during these two bit times. For a Read operation, the MDIO pin must be placed into High-Impedance during these two bit times. The chip will drive the MDIO pin to "0" during the second bit time.

Data. The last 16 bits of the frame are the actual data bits. For a Write operation, these bits are sent to the BCM5201/5202. For a Read operation, these bits are driven by the BCM5201/5202. In either case, the MSB is transmitted first.

When writing to the BCM5201/5202, the data field bits must be stable 10 ns before the rising-edge of MDC, and must be held valid for 10 ns after the rising edge of MDC. When reading from the BCM5201/5202, the data field bits are valid after the rising edge of MDC until the next rising-edge of MDC.

Idle. A high impedance state of the MDIO line. All drivers are disabled and the PHYs pull-up resistor pulls the line high. Following are two examples of MII write and read instructions:

In order to put a chip with PHY address 00001 into Loopback mode, the following MII write instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111
0101 00001 00000 10 0100 0000 0000 0000

In order to determine if a PHY is in the link pass state, the following MII read instruction must be issued:

1111 1111 1111 1111 1111 1111 1111 1111
0110 00001 00001 ZZ ZZZZ ZZZZ ZZZZ ZZZZ

For the MII read operation, the BCM5201/5202 will drive the MDIO line during the TA and Data fields (the last 17 bit times).

MII REGISTER MAP SUMMARY

Table 7 contains the MII register summary for the BCM5201/5202. The register addresses are specified in hex form, and the name of register bits have been abbreviated. When writing to the reserved bits, always write a "0" value, and when reading from these bits, ignore the output value. Never write any value to an undefined register address. The reset value of the registers are shown in the INIT column.

Table 7: MII Register Map Summary

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
00h	**CONTROL**	Soft Reset	Loopback	Force100	AutoNeg Enable	Power Down	Isolate	Restart AutoNeg	Full Duplex	Collision Test	Reserved							3000h
01h	**STATUS**	T4 Capable	TX FDX Capable	TX Capable	10BT FDX Capable	10BT Capable	Reserved				Pream Suppress	AutoNeg Complete	Remote Fault	AutoNeg Capable	Link Status	Jabber Detect	Extd Reg Capable	7809h
02h	**PHYID HIGH**	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0040h
03h	**PHYID LOW**	0	1	1	0	0	0	1	0	0	Model # 0	0	1	0	Revision # 0 0	1	0	6212
04h	**AUTONEG ADVERTISE**	Next Page 0	Reserved	Remote Fault	Reserved Technologies		Pause	Adv T4	Adv TX FDX	Adv TX	Adv BT FDX	Adv BT	0	Advertised Selector Field [4:0] 0 0			1	01E1h
05h	**LINK PARTNER ABILITY**	LP Next Page	LP Acknowl-edge	LP Rmt Fault	Reserved Technologies		LP Pause	LP T4	LP TX FDX	LP TX	LP BT FDX	LP BT	Link Partner Selector Field [4:0]					0000h
06h	**AUTONEG EXPANSION**	Reserved											ParDet Fault	LP Next Pg Able	Next Pg Able	Page Rcvd	LP Auto Neg Able	0000h
07h	**NEXT PAGE**	Reserved																0000h
10h	**100BASE-X AUX CONTROL**	Reserved		Transmit Disable	Reserved		Bypass 4B5B Enc/Dec	Bypass Scram/ Descram	Bypass NRZI Enc/Dec	Bypass Receive Symbol Alignment	Baseline Wander Correct Disable	FEF Enable	Reserved					0000h
11h	**100BASE-X AUX STATUS**	Reserved					FX Mode	Locked	Current 100 Link Status	Current Remote Fault	Reserved	False Carrier Detected	Bad ESD Detected	RCV Error Detected	XMT Error Detected	Lock Error Detected	MLT3 Error Detected	
12h	**100BASE-X RCV ERROR COUNTER**	Reserved										Receive Error Counter						0000h
13h	**100BASE-X FALSE CARRIER COUNTER**	Reserved										False Carrier Sense Counter						0000h

Table 7: MII Register Map Summary (Continued)

ADDR	NAME	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	INIT
14h	**100BASE-X DISCONNECT COUNTER**	Reserved								Disconnect Counter								0000h
15h	**TX EQUALIZER COEFFICIENT Read/Write**	Reserved		Equalizer Coefficient														
16h	**TX EQUALIZER COEFFICIENT CONTROL**	Reserved				Coefficient Select				Reserved		Freeze FFE	Freeze DFE	Reserved	Equalizer Init	Reserved		
17h	**PTEST**	Reserved																0000h
18h	**AUXILIARY CONTROL/ STATUS**	Jabber Disable	Force Link	Reserved					TXDAC Power Mode	HSQ	LSQ	Edge Rate [1:0]		AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	003xh
19h	**AUXILIARY STATUS SUMMARY**	AutoNeg Complete	AutoNeg Complete Ack	AutoNeg Ack Detect	AutoNeg Ability Detect	AutoNeg Pause	AutoNeg HCD			AutoNeg ParDet Fault	LP Remote Fault	LP Page Rcvd	LP AutoNeg Able	SP100 Indicator	Link Status	Internal AutoNeg Enabled	Jabber Detect	0000h
1Ah	**INTERRUPT**	FDX LED Enable	INTR Enable			FDX Mask	SPD Mask	LINK Mask	INTR Mask					FDX Change	SPD Change	Link Change	INTR Status	000xh
1Bh	**AUXILIARY MODE 2**	Reserved						Block RXDV Mode	AutoNeg PDQ Mode	Reserved	Traffic Meter LED	Force LED On	HSTR Mode	Auto LowPwr Mode	Two LNKLED Mode	SQE Disable	Reserved	FF00h
1Ch	**10BASE-T AUX. ERROR & GENERAL STATUS**	Reserved					Manches-ter Code Err (BT)	EOF Err (BT)	Polarity Err (BT)	0	0	1	Reserved	AutoNeg Enable Indicator	Force 100 Indicator	SP100 Indicator	FDX Indicator	002xh
1Dh	**AUXILIARY MODE**	Reserved											Activity LED Disable	Link LED Disable	Reserved	Block TXEN Mode	Reserved	0000h
1Eh	**AUXILIARY MULTI-PHY**	HCD TX FDX	HCD T4	HCD TX	HCD 10BT FDX	HCD 10BT	Reserved		Restart AutoNeg	AutoNeg Complete	Complete ACK	ACK Detect	Ability Detect	Super Isolate	Reserved	10Base-T Serial Mode	Reserved	0000h
1Fh	**BROADCOM Test**	Reserved																

MII CONTROL REGISTER

The MII control register bit descriptions are shown in Table 8.

Table 8: MII Control Register (Address 00000b, 0d, 00h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Reset	R/W (SC)	1 = PHY reset 0 = normal operation	0
14	Loopback	R/W	1 = loopback mode 0 = normal operation	0
13	Forced Speed Selection	R/W	1 = 100 Mbit/s 0 = 10 Mbit/s	1
12	Auto-Negotiation Enable	R/W	1 = Auto-Negotiation enable 0 = Auto-Negotiation disable	1
11	Power Down	RO	0 = normal operation	0
10	Isolate	R/W	1 = electrically isolate PHY from MII 0 = normal operation	0
9	Restart Auto-Negotiation	R/W (SC)	1 = restart Auto-Negotiation process 0 = normal operation	0
8	Duplex Mode	R/W	1 = full-duplex 0 = half-duplex	0
7	Collision Test Enable	R/W	1 = enable the collision test mode 0 = disable the collision test mode	0
6:0	Reserved	RO	Ignore when Read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

RESET. In order to reset the BCM5201/5202 by software control, a “1” must be written to bit 15 of the Control Register using an MII write operation. The bit clears itself after the reset process is complete, and need not be cleared using a second MII write. Writes to other Control Register bits will have no effect until the reset process is completed, which requires approximately 1 µs. Writing a “0” to this bit has no effect. Since this bit is self-clearing, within a few cycles after a write operation, it will return a “0” when read.

LOOPBACK. The BCM5201/5202 may be placed into loopback mode by writing a “1” to bit 14 of the Control Register. The loopback mode may be cleared by writing a “0” to bit 14 of the control register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in loopback mode, otherwise it will return a “0”.

FORCED SPEED SELECTION. If Auto-Negotiation is enabled (both Auto-Negotiation pin and bit are enabled) or disabled by hardware control (Auto-Negotiation pin is pulled-low), this bit has no effect on the speed selection. However, if Auto-Negotiation is disabled by software control, the operating speed of the BCM5201/5202 can be forced by writing the appropriate value to bit 13 of the Control Register. Writing a “1” to this bit forces 100BASE-X operation, while writing a “0” forces 10BASE-T operation. When this bit is read, it returns the value of the software-controlled forced speed selection only. In order to read the overall state of forced speed selection, including both hardware and software control, use bit 2 of the Auxiliary Control Register (18h).

AUTO-NEGOTIATION ENABLE. Auto-Negotiation can be disabled by one of two methods: hardware or software control. If the ANEN input pin is driven to a logic “0”, Auto-Negotiation is disabled by hardware control. If bit 12 of the Control Register is written with a value of “0”, Auto-Negotiation is disabled by software control. When Auto-Negotiation is disabled in this manner, writing a “1” to the same bit of the Control Register or resetting the chip will re-enable Auto-Negotiation. Writing to this bit has no effect when Auto-Negotiation has been disabled by hardware control. When read, this bit will return the value most recently written to this location, or “1” if it has not been written since the last chip reset.

POWER DOWN. The power modes of the BCM5201/5202 are not accessible by this MII register bit. Use LOWPWR pin control instead.

ISOLATE. The PHY may be isolated from its Media Independent Interface by writing a “1” to bit 10 of the Control Register. All MII outputs will be tri-stated and all MII inputs will be ignored. Since the MII management interface is still active, the isolate mode may be cleared by writing a “0” to bit 10 of the control register, or by resetting the chip. When this bit is read, it will return a “1” when the chip is in isolate mode, otherwise it will return a “0”.

RESTART AUTO-NEGOTIATION. Bit 9 of the Control Register is a self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the Auto-Negotiation state machine. In order for this bit to have an effect, Auto-Negotiation must be enabled. Writing a “1” to this bit restarts the Auto-Negotiation, while writing a “0” to this bit has no effect. Since the bit is self-clearing after only a few cycles, it always returns a “0” when read. The operation of this bit is identical to bit 8 of the Auxiliary Multiple PHY Register (1Eh).

DUPLEX MODE. By default, the BCM5201 powers up in half-duplex mode. The chip can be forced into full-duplex mode by writing a “1” to bit 8 of the Control Register while Auto-Negotiation is disabled. Half-Duplex mode can be resumed by writing a “0” to bit 8 of the control register, or by resetting the chip.

COLLISION TEST. The COL pin may be tested by activating the Collision Test mode. While in this mode, asserting TXEN will cause the COL output to go high within 512 bit times. Deasserting TXEN will cause the COL output to go low within 4 bit times. Writing a “1” to bit 7 of the Control Register enables the Collision Test mode. Writing a “0” to this bit or resetting the chip disables the Collision Test mode. When this bit is read, it will return a “1” when the Collision Test mode has been enabled, otherwise it will return a “0”. This bit should only be set while in loopback test mode.

RESERVED BITS. All reserved MII register bits must be written as “0” at all times. Ignore the BCM5201/5202 output when these bits are read.

MII STATUS REGISTER

The MII status register bit descriptions are shown in Table 9.

Table 9: MII Status Register (Address 00001B, 01d, 01h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	100BASE-T4 Capability	RO	0 = Not 100BASE-T4 capable	0
14	100BASE-TX FDX Capability	RO	1 = 100BASE-TX full-duplex capable	1
13	100BASE-TX Capability	RO	1 = 100BASE-TX half-duplex capable	1
12	10BASE-T FDX Capability	RO	1 = 10BASE-T full-duplex capable	1
11	10BASE-T Capability	RO	1 = 10BASE-T half-duplex capable	1
10:7	Reserved	RO	Ignore when Read Ignore when Read	0
6	MF Preamble Suppression	R/W	1 = Preamble may be suppressed 0 = Preamble always required	0
5	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed 0 = Auto-Negotiation process not completed	0
4	Remote Fault	RO	1 = Far-end fault condition detected 0 = No far-end fault condition detected	0
3	Auto-Negotiation Capability	RO	1 = Auto-Negotiation capable 0 = Not Auto-Negotiation capable	1
2	Link Status	RO LL	1 = Link is up (Link Pass state) 0 = Link is down (Link Fail state)	0
1	Jabber Detect	RO LL	1 = Jabber condition detected 0 = No jabber condition detected	0
0	Extended Capability	RO	1 = Extended register capable	1

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

100BASE-T4 CAPABILITY. The BCM5201/5202 is not capable of 100BASE-T4 operation, and will return a “0” when bit 15 of the status register is read.

100BASE-X FULL-DUPLEX CAPABILITY. The BCM5201/5202 is capable of 100BASE-X full-duplex operation, and will return a “1” when bit 14 of the Status Register is read.

100BASE-X HALF-DUPLEX CAPABILITY. The BCM5201/5202 is capable of 100BASE-X half-duplex operation, and will return a “1” when bit 13 of the Status Register is read.

10BASE-T FULL-DUPLEX CAPABILITY. The BCM5201/5202 is capable of 10BASE-T full-duplex operation, and will return a “1” when bit 12 of the Status Register is read.

10BASE-T HALF-DUPLEX CAPABILITY. The BCM5201/5202 is capable of 10BASE-T half-duplex operation, and will return a “1” when bit 11 of the Status Register is read.

RESERVED BITS. Ignore the BCM5201/5202 output when these bits are read.

PREAMBLE SUPPRESSION. This bit is the only writable bit in the Status Register. Setting this bit to a “1” allows subsequent MII management frames to be accepted with or without the standard preamble pattern. When Preamble Suppression is enabled, only 2 preamble bits are required between successive Management Commands, instead of the normal 32.

AUTO-NEGOTIATON COMPLETE. Will return a “1” if Auto-Negotiation process has been completed and the contents of registers 4, 5, and 6 are valid.

REMOTE FAULT. The PHY will return a “1” on bit 4 of the status register when its link partner has signalled a far-end fault condition. When a far-end fault occurs, the bit will be latched at “1” and remain so until the register is read and the remote fault condition has been cleared.

AUTO-NEGOTIATION CAPABILITY. The BCM5201/5202 is capable of performing IEEE Auto-Negotiation, and will return a “1” when bit 4 of the Status Register is read, regardless of whether or not the Auto-Negotiation function has been disabled.

LINK STATUS. The BCM5201/5202 will return a “1” on bit 2 of the Status Register when the link state machine is in Link Pass, indicating that a valid link has been established. Otherwise, it will return “0”. When a link failure occurs after the Link Pass state has been entered, the Link Status bit will be latched at “0” and remain so until the bit is read. After the bit is read, it becomes “1” when the Link Pass state is entered again.

JABBER DETECT. 10BASE-T operation only. The BCM5201/5202 will return a “1” on bit 1 of the Status Register if a jabber condition has been detected. After the bit is read once, or if the chip is reset, it reverts to “0”.

EXTENDED CAPABILITY. The BCM5201/5202 supports extended capability registers, and will return a “1” when bit 0 of the Status Register is read. Several extended registers have been implemented in the BCM5201/5202, and their bit functions are defined later in this section.

PHY IDENTIFIER REGISTERS

The physical indentifier registers bit descriptions are shown in Table 10.

Table 10: PHY Indentifier Registers (Addresses 00010 and 00011b, 02 and 03b, 02 and 03h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*VALUE*
15:0	MII Address 02h	RO	PHYID HIGH	0040h
15:0	MII Address 03h	RO	PHYID LOW	6212h

Broadcom Corporation has been issued an Organizationally Unique Identifier (OUI) by the IEEE. It is a 24 bit number, 00-10-18, expressed as hex values. That number, along with the Broadcom Model Number for the BCM5201/5202 part, 21h, and Broadcom Revision number, 01h for the B0 Rev and 02h for the B1 Rev, is placed into two MII Registers. The translation from OUI, Model Number and Revision Number to PHY Identifier Register occurs as follows:

PHYID HIGH [15:0] = OUI[21:6]

PHY LOW [15:0] = OUI[5:0] + MODEL[5:0] + REV[3:0]

Note: The two most significant bits of the OUI are not represented (OUI[23:22]).

Table 10 shows the result of concatenating these values to form MII Identifier Registers PHYID HIGH and PHYID LOW.

AUTO-NEGOTIATION ADVERTISEMENT REGISTER

Table 11 shows the auto-negotiation advertisement register bit descriptions.

Table 11: Auto-Negotiation Advertisement Register (Address 00100b, 4d, and 04h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Next Page	R/W	(not implemented)	0
14	Reserved	RO	Ignore when Read	
13	Remote Fault	R/W	1 = Transmit Remote Fault	0
12:11	Reserved Technologies	RO	Ignore when Read	
10	Advertise Pause Capability	R/W	1 = Pause Operation for Full-Duplex	0
9	Advertise 100BASE-T4	R/W	0 = Do Not Advertise T4 Capability	0
8	Advertise 100BASE-X FDX	R/W	1 = Advertise 100BASEX Full-Duplex 0 = Do Not Advertise 100BASE-X Full-Duplex	1 If RPTR = 0 0 If RPTR = 1
7	Advertise 100BASE-X	R/W	1 = Advertise 100BASE-X	1
6	Advertise 10BASE-T FDX	R/W	1 = Advertise 10BASE-T Full-Duplex 0 = Do Not Advertise 10BASE-T Full-Duplex	1 If RPTR = 0 0 If RPTR = 1
5	Advertise 10BASE-T	R/W	1 = Advertise 10BASE-T	1
4:0	Advertise Selector Field	RO	Fixed value: indicates 802.3	00001

NEXT PAGE. The BCM5201/5202 does not implement the Next Page function. Thus, bit 15 of the Advertisement Register must always be written “0”.

REMOTE FAULT. Writing a “1” to bit 13 of the Advertisement Register causes a Remote Fault indicator to be sent to the Link Partner during Auto-Negotiation. Writing a “0” to this bit or resetting the chip clears the Remote Fault transmission bit. This bit returns the value last written to it, or else “0” if no write has been completed since the last chip reset.

RESERVED BITS. Ignore output when read.

PAUSE OPERATION FOR FULL-DUPLEX LINKS. The use of this bit is independent of the negotiated data rate, medium, or link technology. The setting of this bit indicates the availability of additional DTE capability when full-duplex operation is in use. This bit is used by one MAC to communicate Pause Capability to its Link Partner and has no effect on PHY operation.

ADVERTISEMENT BITS. Bits 9:5 of the Advertisement Register allow the user to customize the ability information transmitted to the Link Partner. The default value for each bit reflects the abilities of the BCM5201/5202. By writing a “1” to any of the bits, the corresponding ability will be transmitted to the Link Partner. Writing a “0” to any bit causes the corresponding ability to be suppressed from transmission. Resetting the chip restores the default bit values. Reading the register returns the values last written to the corresponding bits, or else the default values if no write has been completed since the last chip reset.

SELECTOR FIELD. Bits 4:0 of the Advertisement register contain the fixed value “00001”, indicating that the chip belongs to the 802.3 class of PHY transceivers.

AUTO-NEGOTIATION LINK PARTNER (LP) ABILITY REGISTER

Table 12 shows the auto-negotiation link partner ability register bit descriptions.

Table 12: Auto-Negotiation Link Partner Ability Register (Address 00101b, 5d, 05h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	LP Next Page	RO	Link Partner next page bit	0
14	LP Acknowledge	RO	Link Partner acknowledge bit	0
13	LP Remote Fault	RO	Link Partner remote fault indicator	0
12:11	Reserved Technologies	RO	Ignore when Read	000
10	LP Pause Operation	RO	Link Partner has Pause Capability	0
9	LP Advertise 100BASE-T4	RO	Link Partner has 100BASE-T4 capability	0
8	LP Advertise 100BASE-X FDX	RO	Link Partner has 100BASE-X FDX capability	0
7	LP Advertise 100BASE-X	RO	Link Partner has 100BASE-X capability	0
6	LP Advertise 10BASE-T FDX	RO	Link Partner has 10BASE-T FDX capability	0
5	LP Advertise 10BASE-T	RO	Link Partner has 10BASE-T capability	0
4:0	Link Partner Selector Field	RO	Link Partner selector field	00000

Note: The values contained in the Auto-Negotiation Link Partner Ability Register are only guaranteed to be valid once Auto-Negotiation has successfully completed, as indicated by bit 5 of the MII Status Register.

NEXT PAGE. Bit 15 of the Link Partner Ability Register returns a value of “1” when the Link Partner implements the Next Page function and has Next Page information that it wants to transmit. The BCM5201/5202 does not implement the Next Page function, and thus ignores the Next Page bit, except to copy it to this register.

ACKNOWLEDGE. Bit 14 of the Link Partner Ability Register is used by the Auto-Negotiation to indicate that a device has successfully received its Link Partner’s Link Code Word.

REMOTE FAULT. Bit 13 of the Link Partner Ability Register returns a value of “1” when the Link Partner signals that a remote fault has occurred. The BCM5201 simply copies the value to this register and does not act upon it.

RESERVED BITS. Ignore when Read.

PAUSE. Indicates that the link partners pause operation is capable.

ADVERTISEMENT BITS. Bits 9:5 of the Link Partner Ability Register reflect the abilities of the Link Partner. A “1” on any of these bits indicates that the Link Partner is capable of performing the corresponding mode of operation. Bits 9:5 are cleared any time Auto-Negotiation is restarted or the BCM5201/5202 is reset.

SELECTOR FIELD. Bits 4:0 of the Link Partner Ability Register reflect the value of the Link Partner’s selector field. These bits are cleared any time Auto-Negotiation is restarted or the chip is reset.

AUTO-NEGOTIATION EXPANSION REGISTER

Table 13 shows the auto-negotiation expansion register bit descriptions.

Table 13: Auto-Negotiation Expansion Register (Address 00110b, 6d, 06h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:5	Reserved	RO	Ignore when Read	
4	Parallel Detection Fault	RO LH	1 = Parallel Detection fault. 0 = No Parallel Detection fault	0
3	Link Partner Next Page Able	RO	1 = Link Partner has Next Page capability 0 = Link Partner does not have Next Page	0
2	Next Page Able	RO	0 = BCM5201/5202 does not have Next Page capability	0
1	Page Received	RO	1 = New page has been received 0 = New page has not been received	0
0	Link Partner Auto-Negotiation Able	RO LH	1 = Link Partner has Auto-Negotiation capability 0 = Link Partner does not have Auto-Negotiation	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

PARALLEL DETECTION FAULT. Bit 4 of the Auto-Negotiation Expansion Register is a read-only bit that gets latched high when a parallel detection fault occurs in the Auto-Negotiation state machine. For further details, please consult the IEEE standard. The bit is reset to “0” after the register is read, or when the chip is reset.

LINK PARTNER NEXT PAGE ABLE. Bit 3 of the Auto-Negotiation Expansion Register returns “1” when the Link Partner has Next Page capabilities. It has the same value as bit 15 of the Link Partner Ability Register.

NEXT PAGE ABLE. The BCM5201/5202 does not have Next Page capabilities, thus it always returns “0” when bit 2 of the Auto-Negotiation Expansion Register is read.

PAGE RECEIVED. Bit 1 of the Auto-Negotiation Expansion Register is latched high when a new Link Code Word is received from the Link Partner, checked, and acknowledged. It remains high until the register is read, or until the chip is reset.

LINK PARTNER AUTO-NEGOTIATION ABLE. Bit 0 of the Auto-Negotiation Expansion Register returns a “1” when the Link Partner is known to have Auto-Negotiation capability. Before any Auto-Negotiation information is exchanged, or if the Link Partner does not comply with IEEE Auto-Negotiation, the bit returns a value of “0”.

AUTO-NEGOTIATION NEXT PAGE REGISTER

The BCM5201/5202 does not implement the Next Page function, and thus the Next Page Transmit Register is not accessible. See Table 14 for the bit description.

Table 14: Next Page Transmit Register (Address 00111b, 7d, 07h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:0	Reserved	RO	(not implemented)	

100BASE-X AUXILIARY CONTROL REGISTER

The 100BASE-X auxiliary control register bit descriptions are shown in Table 15.

Table 15: 100BASE-X Auxiliary Control Register (Address 10000b, 16d, 10h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:14	Reserved	RO	Ignore when Read	
13	Transmit Disable	R/W	1 = Transmitter Disabled in PHY 0 = Normal Operation	0
12:11	Reserved	RO	Ignore when Read	
10	Bypass 4B5B Encoder/ Decoder	R/W	1 = Transmit and Receive 5B codes over MII pins 0 = Normal MII interface	0
9	Bypass Scrambler/ Descrambler	R/W	1 = Scrambler and Descrambler disabled 0 = Scrambler and Descrambler enabled	0
8	Bypass NRZI Encoder/ Decoder	R/W	1 = NRZI Encoder and Decoder disabled 0 = NRZI Encoder and Decoder enabled	0
7	Bypass Receive Symbol Alignment	R/W	1 = 5B Receive Symbols not Aligned 0 = Receive Symbols Aligned to 5B boundaries	0
6	Baseline Wander Correction Disable	R/W	1 = Baseline Wander Correction disabled 0 = Baseline Wander Correction enabled	0
5	FEF Enable	R/W	1 = Far End Fault enabled. 0 = Far End Fault disabled.	0
4:0	Reserved	R/W	Ignore when Read	

TRANSMIT DISABLE. The transmitter may be disabled by writing a “1” to bit 13 of MII Register 10h. The transmitter output (TD±) will be forced into a high impedance state.

BYPASS 4B5B ENCODER/DECODER. The 4B5B encoder and decoder may be bypassed by writing a “1” to bit 10 of MII Register 10h. The transmitter will send 5B codes from the TXER and TXD[3:0] pins directly to the scrambler. TXEN will be ignored and frame encapsulation (insertion of J/K and T/R codes) will not be performed. The receiver will place de-scrambled and aligned 5B codes onto the RXER and RXD[3:0] pins. CRS will still be asserted when a valid frame is received.

BYPASS SCRAMBLER/DESCRAMBLER. The stream cipher function may be disabled by writing a “1” to bit 9 of MII register 10h. The stream cipher function may be re-enabled by writing a “0” to this bit.

BYPASS NRZI ENCODER/DECODER. The NRZI encoder and decoder may be bypassed by writing a “1” to bit 8 of MII Register 10h, causing 3-level NRZ data to be transmitted and received on the cable. Normal operation (3-level NRZI encoding and decoding) may be re-enabled by writing a “0” to this bit.

BYPASS RECEIVE SYMBOL ALIGNMENT. Receive symbol alignment may be bypassed by writing a “1” to bit 7 of MII Register 10h. When used in conjunction with the bypass 4B5B encoder/decoder bit, unaligned 5B codes will be placed directly on the RXER and RXD[3:0] pins.

BASELINE WANDER CORRECTION DISABLE. The baseline wander correction circuit may be disabled by writing a “1” to bit 6 of MII register 10h. The BCM5201/5202 will correct for baseline wander on the receive data signal when this bit is cleared.

FEF ENABLE. Controls the Far End Fault mechanism associated with 100BASE-FX operation. A “1” enables the FEF function and a “0” disables it.

RESERVED BITS. The Reserved bits of the 100BASE-X Auxiliary Control Register must be written as “0” at all times. Ignore the BCM5201/5202 outputs when these bits are read.

100BASE-X AUXILIARY STATUS REGISTER

Table 16 shows the 100BASE-X auxiliary status register bit descriptions.

Table 16: 100BASE-X Auxiliary Status Register (Address 10001b, 17d, 11h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:11	Reserved	RO	Ignore when Read	0
10	FX Mode	RO	1 = 100BASE-FX mode 0 = 100BASE-TX or 10BASET mode	PIN
9	Locked	RO	1 = Descrambler locked 0 = Descrambler unlocked	0
8	Current 100BASE-X Link Status	RO	1 = Link pass 0 = Link fail	0
7	Remote Fault	RO	1 = Remote fault detected 0 = No remote fault detected	0
6	Disconnect State	RO	Not Implemented	0
5	False Carrier Detected	RO LH	1 = False carrier detected since last read 0 = No false carrier since last read	0
4	Bad ESD Detected	RO LH	1 = ESD error detected since last read 0 = No ESD error since last read	0
3	Receive Error Detected	RO LH	1 = Receive error detected since last read 0 = No receive error since last read	0
2	Transmit Error Detected	RO LH	1 = Transmit error code received since last read 0 = No transmit error code received since last read	0
1	Lock Error Detected	RO LH	1 = Lock error detected since last read 0 = No lock error since last read	0
0	MLT3 Code Error Detected	RO LH	1 = MLT3 code error detected since last read 0 = No MLT3 code error since last read	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

FX MODE. Returns a value derived from the SD± input pins. Returns “1” when SD± are driven with a valid differential signal level. Returns “0” when both SD+ and SD– are simultaneously driven low. The 100BASE-FX mode must be enabled (latched on LNKLED pin) before the SD± pins are enabled.

LOCKED. The PHY will return a “1” in bit 9 when the de-scrambler is locked to the incoming data stream. Otherwise it will return a “0”.

LINK STATUS. The PHY will return a “1” in bit 8 when the link status is good. Otherwise it will return a “0”.

REMOTE FAULT. The PHY will return a “1” while its link partner is signalling a far-end fault condition. Otherwise it will return a “0”.

DISCONNECT STATE. The BCM5201/5202 does not contain a Carrier Integrity Monitor, so this bit will never be set.

FALSE CARRIER DETECTED. The PHY will return a “1” in bit 5 of the extended status register if a false carrier has been detected since the last time this register was read. Otherwise it will return a “0”.

BAD ESD DETECTED. The PHY will return a “1” in bit 4 if an end of stream delimiter error has been detected since the last time this register was read. Otherwise it will return a “0”.

RECEIVE ERROR DETECTED. The PHY will return a “1” in bit 3 if a packet was received with an invalid code since the last time this register was read. Otherwise it will return a “0”.

TRANSMIT ERROR DETECTED. The PHY will return a “1” in bit 2 if a packet was received with a transmit error code since the last time this register was read. Otherwise it will return a “0”.

LOCK ERROR DETECTED. The PHY will return a “1” in bit 1 if the de-scrambler has lost lock since the last time this register was read. Otherwise it will return a “0”.

MLT3 CODE ERROR DETECTED. The PHY will return a “1” in bit “0” if an MLT3 coding error has been detected in the receive data stream since the last time this register was read. Otherwise it will return a “0”.

100BASE-X RECEIVE ERROR COUNTER

The 100BASE-X receiver error counter will increment each time the BCM5201/5202 receives a non-collision packet containing at least one receive error. The counter will automatically clear itself when read. When the counter reaches its maximum value, FFh, it stops counting Receive Errors until cleared. See Table 17 for the 100BASE-X receive error counter bit descriptions.

Table 17: 100BASE-X Receive Error Counter (Address 10010b, 18d, 012h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Ignore when Read	
7:0	Receive Error Counter	R/W	Number of Non-Collision Packets with Receive Errors since last Read	00h

100BASE-X FALSE CARRIER SENSE COUNTER

The 100BASE-X false carrier sense counter will increment each time the BCM5201/5202 detects a false carrier on the receive input. The counter will automatically clear itself when read. When the counter reaches its maximum value, FFh, it stops counting False Carrier Sense events until cleared. Table 18 shows the 100BASE-X false carrier sense counter bit descriptions.

Table 18: 100BASE-X False Carrier Sense Counter (Address 10011b, 19d, 13h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Ignore when Read	
7:0	False Carrier Sense Counter	R/W	Number of False Carrier Sense Events since last Read	00h

100BASE-X DISCONNECT COUNTER

The BCM5201/5202 does not contain a Carrier Integrity Monitor, so the 100BASE-X disconnect counter will never increment. See Table 19 for the 100BASE-X disconnect counter bit descriptions.

Table 19: 100BASE-X Disconnect Counter (Address 10100b, 20d, 14h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:8	Reserved	RO	Ignore when Read	
7:0	Disconnect Counter	R/W	Not Implemented	00h

PTEST REGISTER

The bit description for the PTEST register is shown in Table 20.

Table 20: PTEST Register (Address 10111b, 23d, 17h)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:0	Reserved	RO	Ignore when Read	

AUXILIARY CONTROL/STATUS REGISTER

The Auxiliary Control/Status register bit descriptions are shown in Table 21.

Table 21: Auxiliary Control/Status Register (Address 11000b, 24d, 18h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Jabber Disable	R/W	1 = Jabber function disabled 0 = Jabber function enabled	0
14	Force Link	R/W	1 = Force 10BASE-T Link Pass 0 = Normal 10BASE-T Link operation	0
13:8	Reserved	RO	Ignore when Read	000000
7:6	HSQ : LSQ	R/W	These two bits define the Squelch Mode of the 10BASE-T Carrier Sense mechanism: 00 = Normal Squelch 01 = Low Squelch 10 = High Squelch 11 = Not Allowed	00
5:4	Edge Rate [1:0]	R/W	00 = 1 ns 01 = 2 ns 10 = 3 ns 11 = 4 ns	11
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	ANEN Pin
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	F100 Pin
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	
0	Full-Duplex Indication	RO	1 = Full-duplex active 0 = Full-duplex not active	FDX Pin

JABBER DISABLE. 10BASE-T operation only. Bit 15 of the Auxiliary Control Register allows the user to disable the Jabber Detect function, defined in the IEEE standard. This function shuts off the transmitter when a transmission request has exceeded a maximum time limit. By writing a “1” to bit 15 of the Auxiliary Control Register, the Jabber Detect function is disabled. Writing a “0” to this bit or resetting the chip restores normal operation. Reading this bit returns the value of Jabber Detect Disable.

LINK FORCE. Writing a “1” to bit 14 of the Auxiliary Control Register allows the user to disable the Link Integrity state machines, and place the BCM5201/5202 into forced Link Pass status. Writing a “0” to this bit or resetting the chip restores the Link Integrity functions. Reading this bit returns the value of the Force Link bit.

HSQ AND LSQ. Extend or decrease the squelch levels for detection of incoming 10BASET data packets. The default squelch levels implemented are those defined in the IEEE standard. The high- and low-squelch levels are useful for situations where the IEEE-prescribed levels are inadequate. The squelch levels are used by the CRS/LINK block to filter out noise and recognize only valid packet preambles and link integrity pulses. Extending the squelch levels allows the BCM5201/5202 to operate properly over longer cable lengths. Decreasing the squelch levels may be useful in situations where there is a high level of noise present on the cables. Reading these two bits returns the value of the squelch levels.

EDGE RATE. Control bits used to program the transmit DAC output edge rate in 100BASE-TX mode. A larger value on these bits produces slower transitions on the transmit waveform.

AUTO-NEGOTIATION INDICATION. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5201/5202. A combination of a “1” in bit 12 of the Control Register and a logic “1” on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Control Register (18h) returns a “0”. At all other times, it returns a “1”.

FORCE100/10 INDICATION. A read-only bit that returns a value of “0” when one of following cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. The ANEN pin is high AND bit 12 of the Control Register has been written “0” AND bit 13 of the Control Register has been written “0”.

When bit 2 of the Auxiliary Control Register (18h) is “0”, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

SPEED INDICATION. A read-only bit that shows the true current operation speed of the BCM5201/5202. A “1” indicates 100BASE-X operation, and a “0” indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5201 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION. A read-only bit that returns a “1” when the BCM5201 is in full-duplex mode. In all other modes, it returns a “0”.

AUXILIARY STATUS SUMMARY REGISTER

The Auxiliary Status Summary Register contains copies of redundant status bits found elsewhere within the MII register space. Descriptions for each of these individual bits can be found associated with their primary register descriptions. Table 22 indicates the bits found in this register.

Table 22: Auxiliary Status Summary Register (Address 11001b, 25d, 19h)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process completed	0
14	Auto-Negotiation Complete Acknowledge	RO LH	1 = Auto-Negotiation completed acknowledge state	0
13	Auto-Negotiation Acknowledge Detected	RO LH	1 = Auto-Negotiation acknowledge detected	0
12	Auto-Negotiation Ability Detect	RO LH	1 = Auto-Negotiation for Link Partner ability	0
11	Auto-Negotiation Pause	RO	BCM5201/5202 & Link Partner pause operation bit	0
10:8	Auto-Negotiation HCD	RO	000 = No Highest Common Denominator 001 = 10BASE-T 010 = 10BASE-T Full-Duplex 011 = 100BASE-TX 100 = 100BASE-T4 101 = 100BASE-TX Full-Duplex 11x = Undefined	000
7	Auto-Negotiation Parallel Detection Fault	RO LH	1 = Parallel Detection Fault	0
6	Link Partner Remote Fault	RO	1 = Link Partner remote fault	0
5	Link Partner Page Received	RO LH	1 = New page has been received	0
4	Link Partner Auto-Negotiation Able	RO	1 = Link Partner is Auto-Negotiation capable	0
3	Speed Indicator	RO	1 = 100 Mbps 0 = 10 Mbps	
2	Link Status	RO LL	1 = Link is up (Link Pass state)	0
1	Auto-Negotiation Enabled	RO	1 = Auto-Negotiation enabled	ANEN pin
0	Jabber Detect	RO LH	1 = Jabber condition detected	0

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

INTERRUPT REGISTER

The Interrupt register bit descriptions are shown in Table 23.

Table 23: Interrupt Register (Address 11010b, 26d, 1Ah)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	FDX LED Enable	R/W	Full-Duplex LED Enable	0
14	INTR Enable	R/W	Interrupt Enable	0
13:12	Reserved	RO	Ignore when Read	0
11	FDX Mask	R/W	Full-Duplex Interrupt Mask	1
10	SPD Mask	R/W	SPEED Interrupt Mask	1
9	LINK Mask	R/W	LINK Interrupt Mask	1
8	INTR Mask	R/W	Master Interrupt Mask	1
7:4	Reserved	RO	Ignore when Read	0
3	FDX Change	RO LH	Duplex Change Interrupt	0
2	SPD Change	RO LH	Speed Change Interrupt	0
1	LINK Change	RO LH	Link Change Interrupt	0
0	INTR Status	RO LH	Interrupt Status	0

FDX LED ENABLE. Setting this bit enables the FDX LED mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time when FDX LED mode is enabled. XMTLED# becomes FDXLED# and RCVLED# becomes ACTLED#.

INTERRUPT ENABLE. Setting this bit enables Interrupt Mode. Bits 14 and 15 of this register are mutually exclusive. Only one may be set at a time. When Interrupt Mode is enabled, XMTLED# becomes INTR# and RCVLED# becomes ACTLED#.

FDX MASK. When this bit is set, changes in Duplex mode will not generate an interrupt.

SPD MASK. When this bit is set, changes in operating speed will not generate an interrupt.

LINK MASK. When this bit is set, changes in Link status will not generate an interrupt.

INTERRUPT MASK. Master Interrupt Mask. When this bit is set, no interrupts will be generated, regardless of the state of the other MASK bits.

FDX CHANGE. A “1” indicates a change of Duplex status since last register read. Register read clears the bit.

SPD CHANGE. A “1” indicates a change of Speed status since last register read. Register read clears the bit.

LINK CHANGE. A “1” indicates a change of Link status since last register read. Register read clears the bit.

INTERRUPT STATUS. Represents status of the INTR# pin. A “1” indicates that the Interrupt Mask is off and that one or more of the change bits are set. Register read clears the bit.

AUXILIARY MODE 2 REGISTER

The bit descriptions for the Auxiliary Mode 2 register are shown in Table 24.

Table 24: Auxiliary Mode 2 (Address 11011b, 27d, 1Bh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:10	Reserved	R/W	Ignore when Read	111111b
9	Block RXDV Mode	R/W	1 = Block RXDV Mode enabled 0 = Block RXDV Mode disabled	1
8	Auto-Neg Parallel Detection Qualification Mode	R/W	1 = Enable Auto-Neg PDQ mode 0 = Disable Auto-Neg PDQ mode	1
7	Reserved	R/W	Ignore when Read	0
6	Traffic Meter LED Mode	R/W	1 = Enable Traffic Meter LED mode 0 = Disable Traffic Meter LED mode	0
5	Force XMTLED, RCVLED On	R/W	1 = Force XMTLED#, RCVLED# on 0 = XMTLED#, RCVLED# normal operation	0
4	High Speed Token Ring Mode	R/W	1 = Enable High Speed Token Ring mode 0 = Disable High Speed Token Ring mode	0
3	Automatic Low Power Mode	R/W	1 = Enable Automatic Low Power mode 0 = Disable Automatic Low Power mode	0
2	Two LNKLED Mode	R/W	1 = Enable Two LNKLED mode 0 = Disable Two LNKLED mode	0
1	SQE Disable	R/W	1 = Disable SQE pulse transmission on COL pin 0 = Enable SQE pulse transmission on COL pin	0
0	Reserved	R/W	Ignore when Read	0

BLOCK RXDV MODE. In this mode, RXDV is blocked from asserting during transmit packets while in 10BASE-T half-duplex mode. This mode is enabled by default.

AUTO-NEGOTIATION PARALLEL DETECTION QUALIFICATION (PDQ) MODE. This mode only allows successful parallel detection when the corresponding advertisement bits are set. For example, if the 10BASE-T advertisement bits are not set, the chip will not parallel detect to 10BASE-T mode. This mode is enabled by default.

TRAFFIC METER LED MODE. This mode dramatically decreases the blink rate of XMTLED# and RCVLED# (or ACTLED#, if appropriate). Thus, the LED will appear brighter when heavy traffic is present, and dimmer for lighter traffic.

FORCE XMTLED, RCVLED ON. When bit 5 of the Aux Mode 2 register is asserted, both XMTLED# and RCVLED# (or ACTLED#, if appropriate) will be asserted (logic “0”).

HIGH SPEED TOKEN RING MODE. The High Speed Token ring mode allows reception of 100BASE-TX packets that are much longer than normally allowed in Ethernet environments. Ordinarily, the scrambler locking state machine requires that an IDLE sequence be present on the receive data stream at least every 727 µs. This translates to a maximum packet length of 9 kB. But Token Ring packets can be much longer than this. By writing a “1” to bit 4 of the Aux Mode 2 register, the High Speed Token Ring mode is enabled, increasing the timeout counter to 5816 µs for a maximum packet length of roughly 72 kB. This mode only affects 100BASE-TX operation.

AUTOMATIC LOW POWER MODE. This mode removes the need for external logic to control the LOWPWR pin when there is no energy detected on the cable. When this mode is enabled, a loss of energy detected on the cable automatically places the chip into Low Power mode. The Energy Detection function continues to operate. When energy is detected again, the chip automatically reverts to full power state.

TWO LNKLED MODE. This mode changes the functions of the SPDLED# and LINKLED# pins. SPDLED# becomes an indicator of valid 10BASE-T link, while LNKLED# becomes an indicator of valid 100BASE-X link. Note that the polarities of these two outputs are still influenced by the FX mode and repeater mode (see definitions of SPDLED# and LNKLED# pins).

SQE DISABLE. Writing a “1” to bit 1 of the Aux Mode 2 register allows the 10BASE-T SQE pulse to be disabled. An SQE pulse is a short pulse on the COL output following the successful transmission of a packet while in 10BASE-T half duplex mode. Note that SQE pulses will be enabled by default.

10BASE-T AUXILIARY ERROR AND GENERAL STATUS REGISTER

The bit descriptions for the 10BASE-T Auxiliary Error and General Status register are shown in Table 25.

Table 25: 10BASE-T Auxiliary Error and General Status Register (Address 11100b, 28d, 1Ch)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:11	Reserved	RO	Ignore when Read	
10	Manchester Code Error	RO LH	1 = Manchester Code Error (10BASE-T)	0
9	EOF Error	RO LH	1 = EOF Detection Error (10BASE-T)	0
8	Polarity Inversion	RO	1 = Channel Polarity Inverted 0 = Channel Polarity Correct	0
7:5	Revision	RO	Revision Number	001
4	Reserved	RO	Ignore when Read	
3	Auto-Negotiation Indication	RO	1 = Auto-Negotiation activated 0 = Speed forced manually	ANEN Pin
2	Force 100/10 Indication	RO	1 = Speed forced to 100BASE-X 0 = Speed forced to 10BASE-T	F100 Pin
1	Speed Indication	RO	1 = 100BASE-X 0 = 10BASE-T	
0	Full-Duplex Indication	RO	1 = Full-Duplex Active 0 = Full-Duplex not Active	FDX Pin

Note: R/W = Read/Write, RO = Read only, SC = Self Clear, LL = latched low, LH = latched high (LL and LH are cleared after read operation)

MANCHESTER CODE ERROR. Indicates that a Manchester code violation was received. This bit is only valid during 10BASE-T operation.

EOF ERROR. Indicates that the EOF (end of frame) sequence was improperly received, or not received at all. This error bit is only valid during 10BASE-T operation.

POLARITY. Reflects the Polarity status of the receive channel pair. The BCM5201/5202 is capable of automatically inverting the polarity of the receive channel. No data errors are reported to indicate that the automatic polarity inversion is occurring. Instead, this bit returns a “1” whenever the polarity of the receive channel is inverted.

REVISION. Read-only bits that return the revision number of the BCM5201/5202. The current revision is labelled “001”.

AUTO-NEGOTIATION INDICATION. A read-only bit that indicates whether Auto-Negotiation has been enabled or disabled on the BCM5201/5202. A combination of a “1” in bit 12 of the Control Register and a logic “1” on the ANEN input pin is required to enable Auto-Negotiation. When Auto-Negotiation is disabled, bit 3 of the Auxiliary Error Register (1Ch) returns a “0”. At all other times, it returns a “1”.

FORCE100/10 INDICATION. A read-only bit that returns a value of “0” when one of the following two cases is true:

1. The ANEN pin is low AND the F100 pin is low.
2. The ANEN pin is high AND bit 12 of the Control Register has been written “0” AND bit 13 of the Control Register has been written “0”.

When bit 2 of the Auxiliary Error Register (1Ch) is “0”, the speed of the chip will be 10BASE-T. In all other cases, either the speed is not forced (Auto-Negotiation is enabled), or the speed is forced to 100BASE-X.

SPEED INDICATION. A read-only bit that shows the true current operation speed of the BCM5201/5202. A “1” indicates 100BASE-X operation, and a “0” indicates 10BASE-T. Note that while the Auto-Negotiation exchange is performed, the BCM5201/5202 is always operating at 10BASE-T speed.

FULL-DUPLEX INDICATION. A read-only bit that returns a “1” when the BCM5201/5202 is in full-duplex mode. In all other modes, it returns a “0”.

AUXILIARY MODE REGISTER

Table 26 shows the bit descriptions for the Auxiliary Mode register.

Table 26: Auxiliary Mode Register (Address 11101b, 29d, 1Dh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15:5	Reserved	RO	Ignore when Read	
4	Activity LED Disable	R/W	1 = Disable XMT/RCV Activity LED outputs 0 = Enable XMT/RCV Activity LED outputs	0
3	Link LED Disable	R/W	1 = Disable Link LED output 0 = Enable Link LED output	0
2	Reserved	RO	Ignore when Read	
1	Block TXEN Mode	R/W	1 = Enable Block TXEN mode 0 = Disable Block TXEN mode	0
0	Reserved	RO	Ignore when Read	0

ACTIVITY LED DISABLE. When set to “1”, disables the XMTLED# and RCVLED# output pins. When “0”, XMTLED# and RCVLED# output pins are enabled.

LINK LED DISABLE. When set to “1”, disables the Link LED output pin. When “0”, Link LED output is enabled.

BLOCK TXEN MODE. When this mode is enabled, short IPGs of 1, 2, 3 or 4 TXC cycles will result in the insertion of two IDLEs before the beginning of the next packet’s JK symbols.

AUXILIARY MULTIPLE PHY REGISTER

The bit descriptions for the Auxiliary Multiple PHY register are shown in Table 27.

Table 27: Auxiliary Multiple PHY Register (Address 11110b, 30d, 1Eh)

BIT	*NAME*	*R/W*	*DESCRIPTION*	*DEFAULT*
15	HCD TX FDX	RO	1 = Auto-Negotiation result is 100BASE-TX full-duplex	0
14	HCD T4	RO	1 = Auto-Negotiation result is 100BASE-T4	0
13	HCD TX	RO	1 = Auto-Negotiation result is 100BASE-TX	0
12	HCD 10BT FDX	RO	1 = Auto-Negotiation result is 10BASE-T full-duplex	0
11	HCD 10BT	RO	1 = Auto-Negotiation result is 10BASE-T	0
10:9	Reserved	RO	Ignore when Read	
8	Restart Auto-Negotiation	R/W (SC)	1 = restart Auto-Negotiation process 0 = (No effect)	0
7	Auto-Negotiation Complete	RO	1 = Auto-Negotiation process Completed 0 = Auto-Negotiation process not Completed	0
6	Acknowledge Complete	RO	1 = Auto-Negotiation Acknowledge Completed	0
5	Acknowledge Detected	RO	1 = Auto-Negotiation Acknowledge Detected	0
4	Ability Detect	RO	1 = Auto-Negotiation waiting for LP Ability	0

Table 27: Auxiliary Multiple PHY Register (Address 11110b, 30d, 1Eh) (Continued)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
3	Super Isolate	R/W	1 = Super Isolate mode 0 = Normal Operation	0
2	Reserved	RO	Ignore when Read	0
1	10BASE-T Serial Mode	R/W	1 = 10BASE-T serial mode 0 = 10BASE-T MII mode	0
0	Reserved	RO	Ignore when Read	0

HCD BITS. Bits 15:11 of the Auxiliary Multiple PHY Register are five read-only bits that report the Highest Common Denominator (HCD) result of the Auto-Negotiation process. Immediately upon entering the Link Pass state after each reset or Restart Auto-Negotiation, only one of these five bits will be "1". The Link Pass state is identified by a "1" in bit 6 or 7 of this register. The HCD bits are reset to "0" every time Auto-Negotiation is restarted or the BCM5201/5202 is reset. Note that for their intended application, these bits will uniquely identify the HCD only after the first Link Pass after reset or restart of Auto-Negotiation. On later Link Fault and subsequent re-negotiations, if the ability of the Link Partner is different, more than one of the above bits may be active.

RESTART AUTO-NEGOTIATION. A self-clearing bit that allows the Auto-Negotiation process to be restarted, regardless of the current status of the state machine. For this bit to work, Auto-Negotiation must be enabled. Writing a "1" to this bit restarts Auto-Negotiation. Since the bit is self-clearing, it always returns a "0" when read. The operation of this bit is identical to bit 9 of the Control Register.

AUTO-NEGOTIATION COMPLETE. This read-only bit returns a "1" after the Auto-Negotiation process has been completed. It remains "1" until the Auto-Negotiation process is restarted, a Link Fault occurs, or the chip is reset. If Auto-Negotiation is disabled or the process is still in progress, the bit returns a "0".

ACKNOWLEDGE COMPLETE. This read-only bit returns a "1" after the Acknowledgment exchange portion of the Auto-Negotiation process has been completed and the Arbitrator state machine has exited the Complete Acknowledge state. It remains this value until the Auto-Negotiation process is restarted, a Link Fault occurs, Auto-Negotiation is disabled, or the BCM5201/5202 is reset.

ACKNOWLEDGE DETECTED. This read-only bit is set to "1" when the Arbitrator state machine exits the Acknowledge Detect state. It remains high until the Auto-Negotiation process is restarted, or the BCM5201/5202 is reset.

ABILITY DETECT. This read-only bit returns a "1" when the Auto-Negotiation state machine is in the Ability Detect state. It enters this state a specified time period after the Auto-Negotiation process begins, and exits after the first FLP burst or link pulses are detected from the Link Partner. This bit returns a "0" any time the Auto-Negotiation state machine is not in the Ability Detect state.

SUPER ISOLATE. Writing a "1" to this bit places the BCM5201/5202 into the Super Isolate mode. Similar to the Isolate mode, all MII inputs are ignored, and all MII outputs are tri-stated. Additionally, all link pulses are suppressed. This allows the BCM5201/5202 to coexist with another PHY on the same adapter card, with only one being activated at any time.

10BASE-T SERIAL MODE. Writing a "1" to bit 1 enables the 10BASE-T Serial mode. In the normal 10BASE-T mode of operation, as defined by the IEEE MII standard, transmit and receive data packets traverse the TXD[3:0] and RXD[3:0] busses at a rate of 2.5 MHz. In the 10BASE-T Serial mode, data packets traverse to the MAC layer using only TXD[0] and RXD[0] at a rate of 10 MHz. Receive and Transmit clocks change to 10 MHz. Serial operation is not available in 100BASE-X mode.

BROADCOM TEST REGISTER

All bits in the Broadcom Test register are reserved as shown in Table 28.

Table 28: Broadcom Test (Address 11111b, 31d, 1Fh)

BIT	NAME	R/W	DESCRIPTION	DEFAULT
15:0	Reserved	RO	Ignore when Read	0

SECTION 6: TIMING AND AC CHARACTERISTICS

The timing information contained in this section applies to the BCM5201 and the BCM5202.

All MII Interface pins comply with IEEE 802.3u timing specifications (see Reconciliation Sublayer and Media Independent Interface in IEEE 802.3u timing specifications). All digital output timing specified at C_L = 30 pF.

Output rise/fall times measured between 10% and 90% of the output signal swing. Input rise/fall times measured between V_{IL} max. and V_{IH} min. Output signal transitions referenced to the midpoint of the output signal swing. Input signal transitions referenced to the midpoint between V_{IL} max. and V_{IH} min. See Table 29 and Table 30 for the timing parameters. See Figure 3 for an illustration of clock and reset timing.

Table 29: Clock Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
XTALI Cycle Time	CK_CYCLE	39.998	40	40.002	ns
XTALI High/Low Time	CK_HI CK_LO	14	20	26	ns
XTALI Rise/Fall Time	CK_EDGE	–	–	4	ns

Table 30: Reset Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
Reset Pulse Length with stable XTALI Input	RESET_LEN	400	–	–	ns
Activity after end of Hardware Reset	RESET_WAIT	100	–	–	µs
RESET# Rise/Fall Time	RESET_EDGE	–	–	10	ns

Figure 3: Clock and Reset Timing

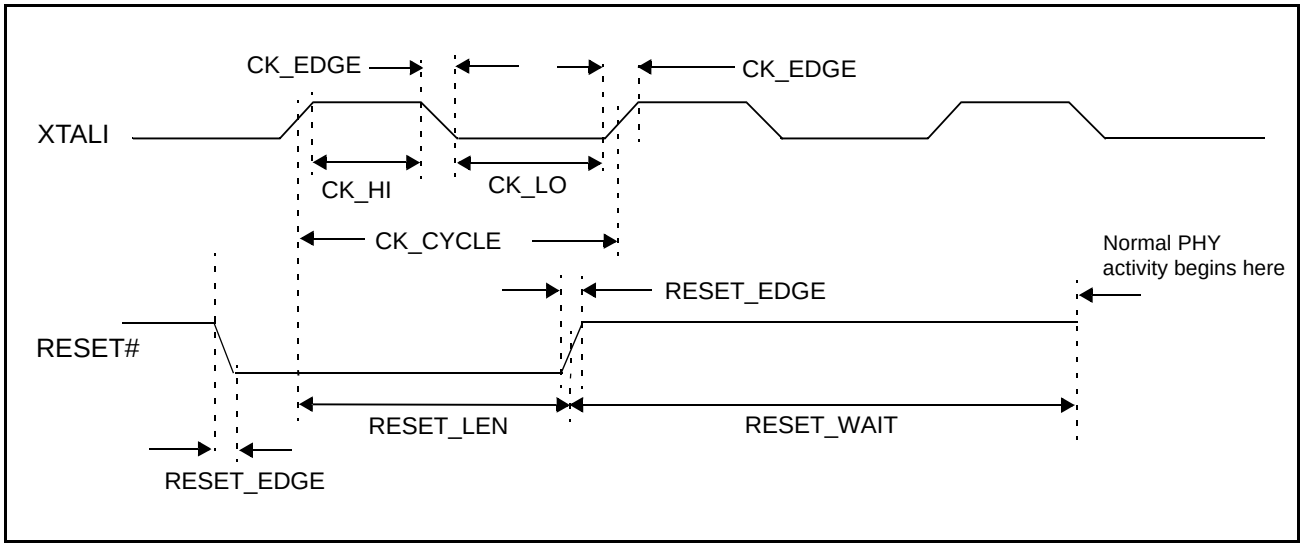


Table 31 provides the parameters for 100BASE-X transmit timing. Figure 4 illustrates the 100BASE-TX transmit start of packet timing and Figure 5 shows the100BASE-TX transmit end of packet timing.

Table 31: 100BASE-X Transmit Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
TXC Cycle Time		–	40	–	ns
TXC High/Low Time		16	20	24	ns
TXC Rise/Fall Time		2	–	5	ns
TXEN, TXD[3:0] Setup Time to TXC rising*	TXEN_SETUP	13.5	–	–	ns
TXEN, TXD[3:0] Hold Time from TXC rising*	TXEN_HOLD	0	–	–	ns
TD± after TXEN Assert	TXEN_TDATA	60	–	80	ns
TXD to TD± Steady State Delay	TXD_TDATA	60	–	80	ns
TD± after TXEN Assert (Repeater Mode)	TXEN_TDATA	30	–	38	ns
TXD to TD± Steady State Delay (Repeater Mode)	TXD_TDATA	30	–	38	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	–	30	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	–	30	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL	–	–	30	ns
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP	–	–	30	ns
TXEN, TXD[3:0] Setup Time to XTALI rising*		2	–	–	ns
TXEN, TXD[3:0] Hold Time from XTALI rising*		10	–	–	ns
* The BCM5201/5202 will function properly if the TXEN, TXER, and TXD[3:0] inputs meet the setup and hold times to either the TXC (DTE Mode) output or the XTALI (Repeater) input.					

Figure 4: Transmit Start of Packet Timing (100BASE-TX)

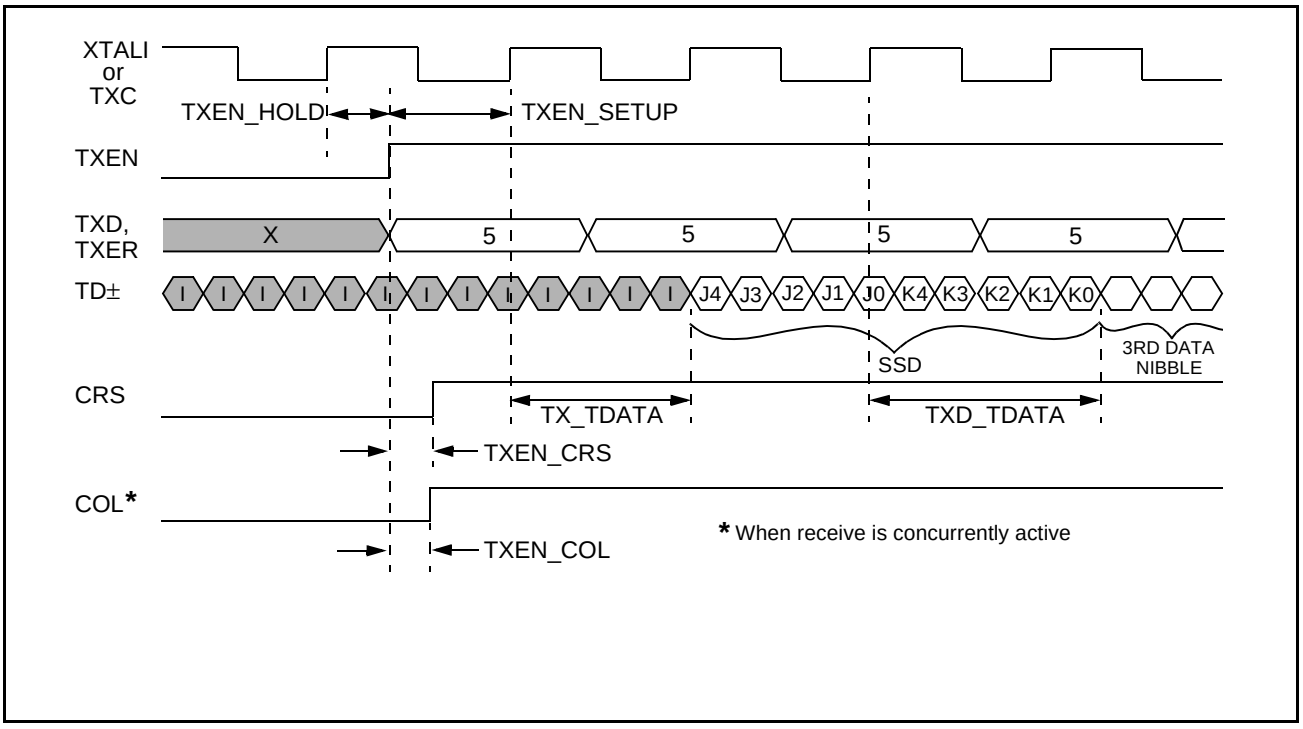


Figure 5: Transmit End of Packet Timing (100BASE-TX)

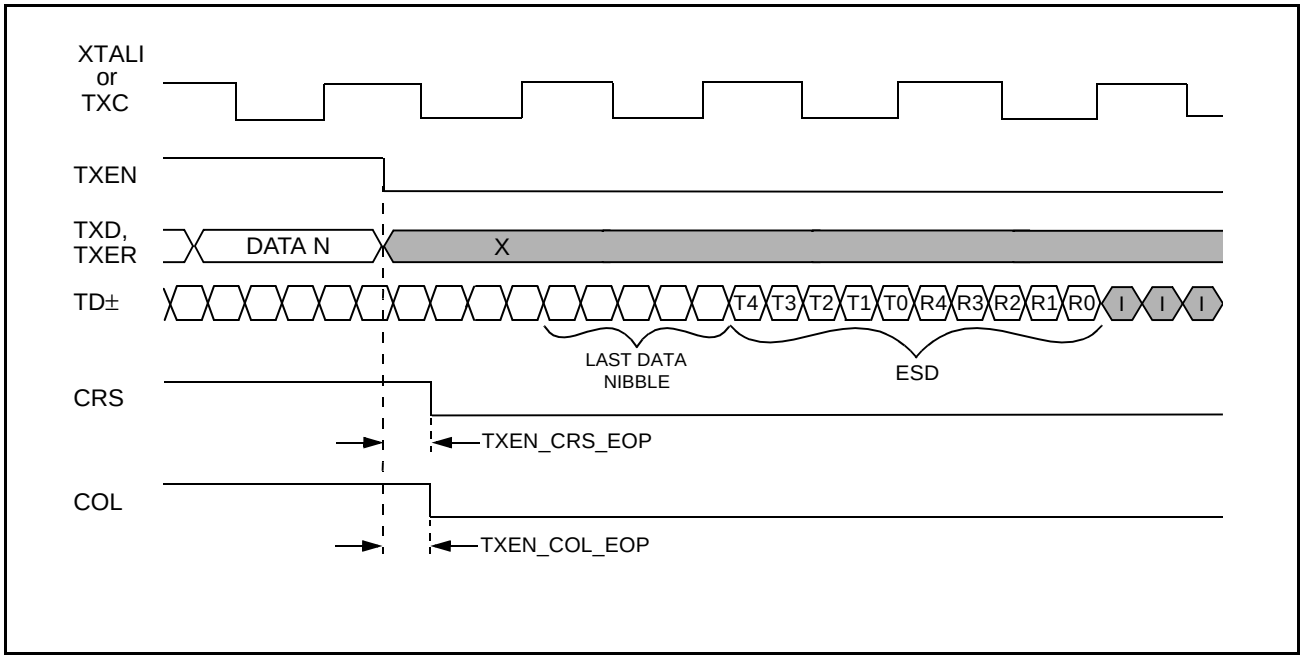


Table 32 provides 10BASE-X receive timing parameters. See Figure 6 and Figure 7 for illustrations of 100BASE-TX receive start of packet timing parameters and 100BASE-TX receive end of packet timing. Figure 8 shows 100BASE-TX receive packet premature end. See Figure 9 for an illustration of link failure or stream cipher error during receive packet. 100BASE-TX False carrier sense timing is shown in Figure 10.

Table 32: 100BASE-X Receive Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
RXC Cycle Time		39.5	40	40.5	ns
RXC High/Low Time (RXDV asserted)		18	20	22	ns
RXC High Time (RXDV deasserted)		18	20	54	ns
RXC Low Time (RXDV deasserted)		18	20	38	ns
RXC Rise/Fall Time		2	–	5	ns
RXDV, RXER, RXD[3:0] Delay from RXC falling		-4	–	4	ns
CRS Deassert from RXC falling (valid EOP only)		-4	–	4	ns
CRS Assert after RD±	RX_CRS	125	–	145	ns
CRS Deassert after RD± (valid EOP)	RX_CRS_EOP	165	–	185	ns
CRS Deassert after RD± (premature end)	RX_CRS_IDLE	170	–	200	ns

Table 32: 100BASE-X Receive Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
RXDV Assert after RD±	RX_RXDV	165	–	185	ns
RXDV Deassert after RD± (valid EOP)	RX_RXDV_EOP	165	–	185	ns
RXDV Assert after CRS		35	–	45	ns
RD± to RXD Steady State Delay	RX_RXD	150	–	180	ns
COL Assert after RD± (while TX)	RX_COL	125	–	145	ns
COL Deassert after RD± (valid EOP)	RX_COL_EOP	165	–	185	ns
COL Deassert after RD± (premature end)	RX_COL_IDLE	170	–	200	ns
RXEN high to RXC, RXDV, RXER, RXD[3:0] Delay		0		50	ns
RXC, RXDV, RXER, RXD[3:0] high-Z from RXEN low		20		70	ns

Note: RXC minimum high and low times are guaranteed when RXEN is asserted or deasserted. The MII port will always tristate while RXEN is low.

Figure 6: Receive Start of Packet Timing (100BASE-TX)

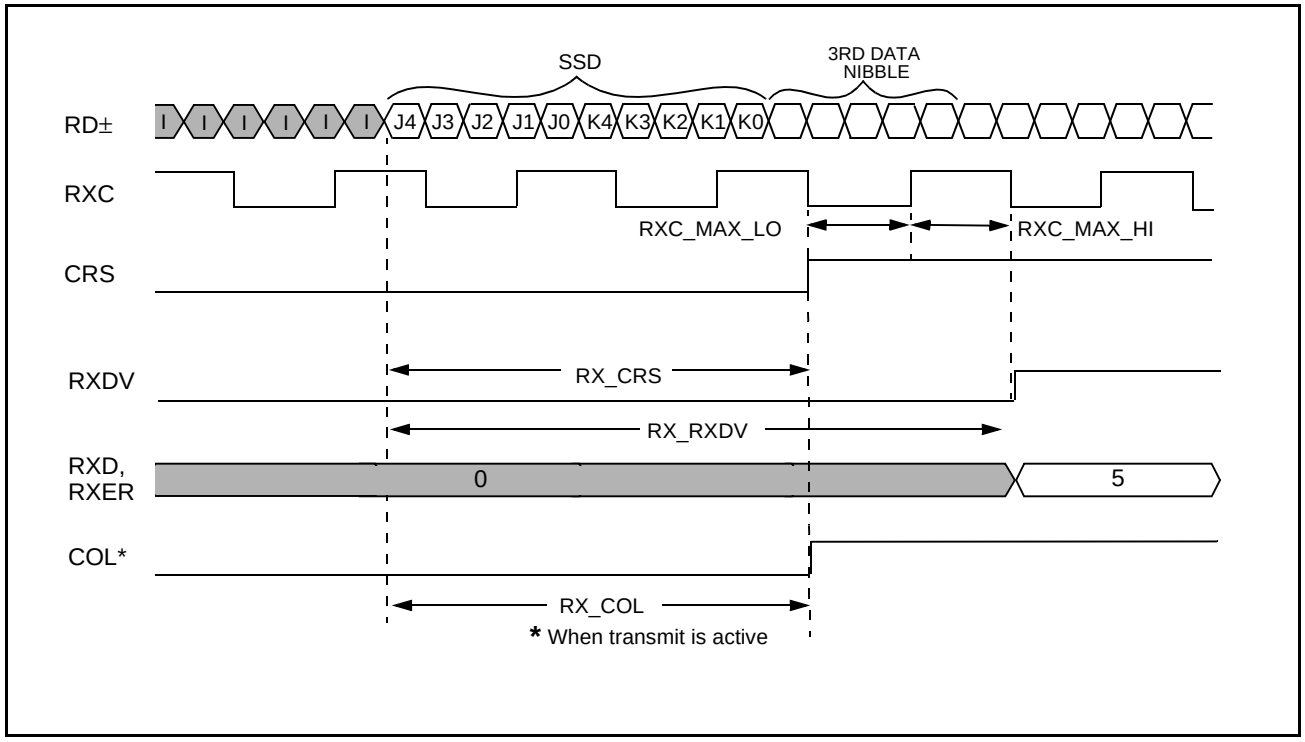


Figure 7: Receive End of Packet Timing (100BASE-TX)

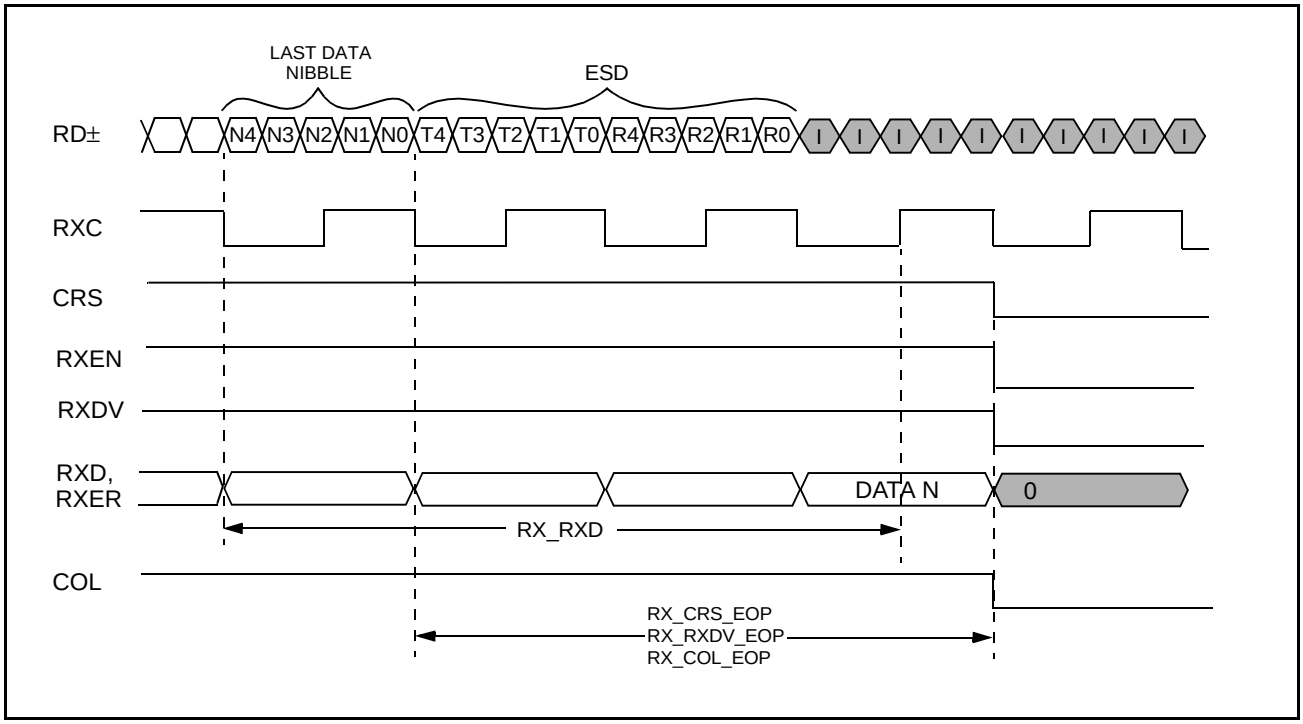


Figure 8: Receive Packet Premature End (100BASE-TX)

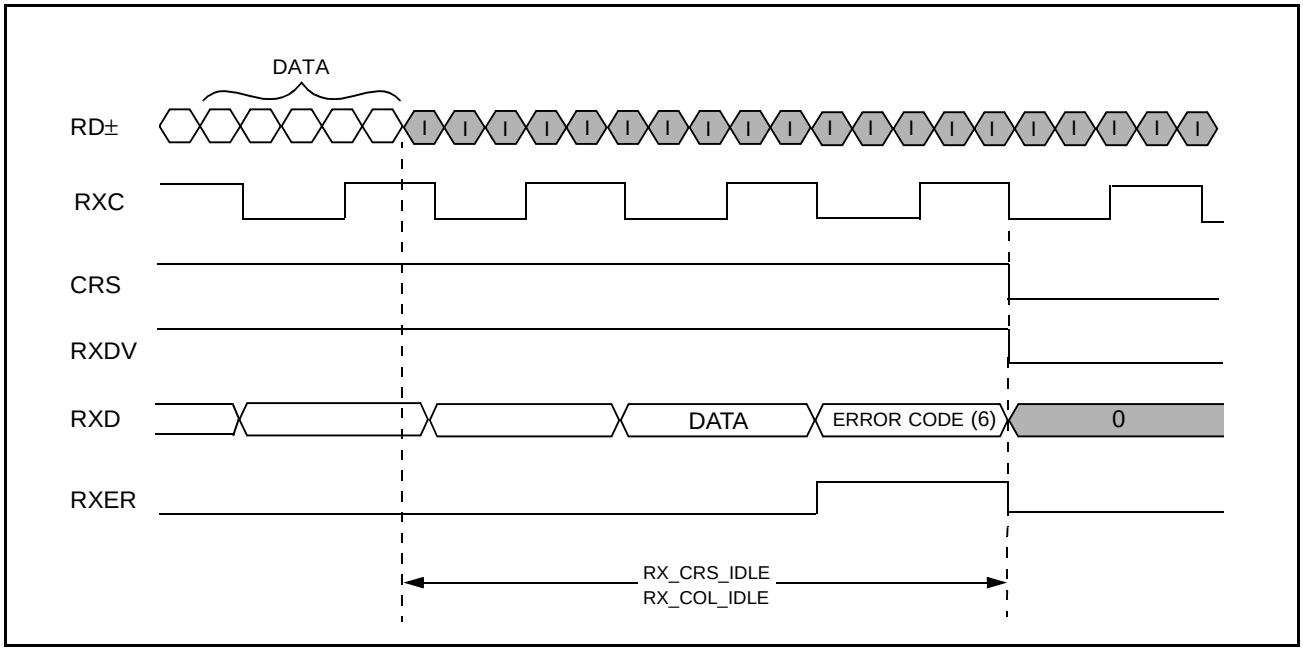


Figure 9: Link Failure or Stream Cipher Error During Receive Packet

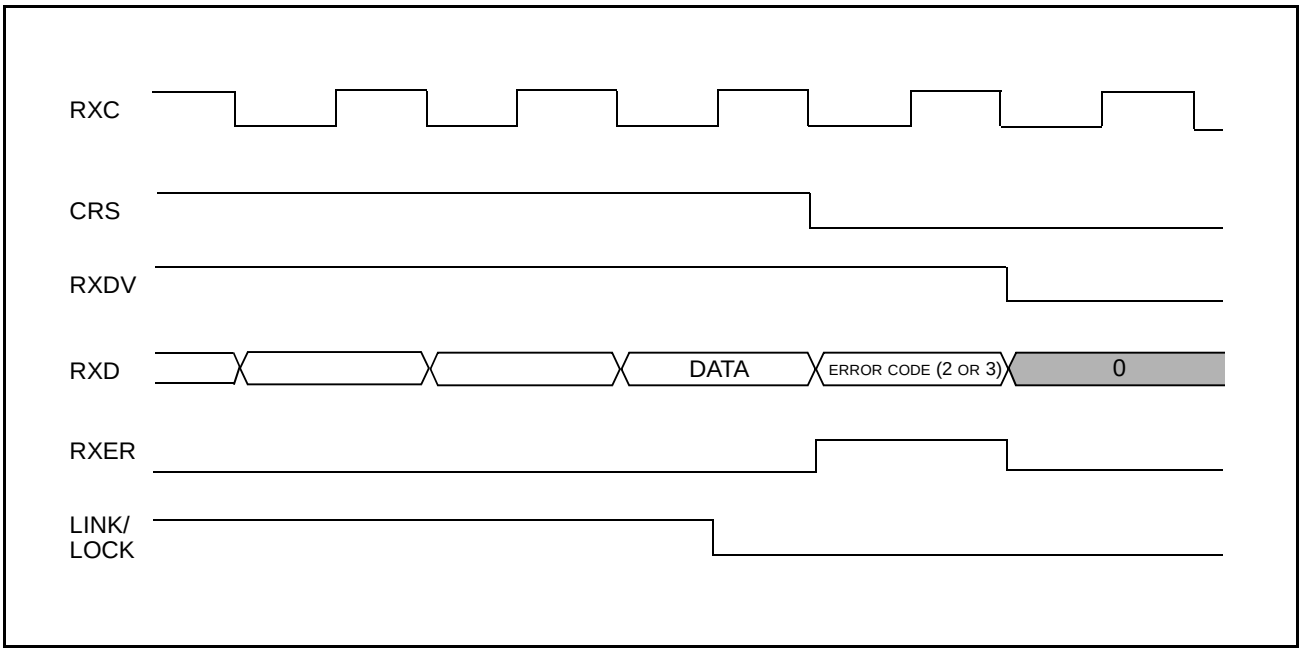


Figure 10: False Carrier Sense Timing (100BASE-TX)

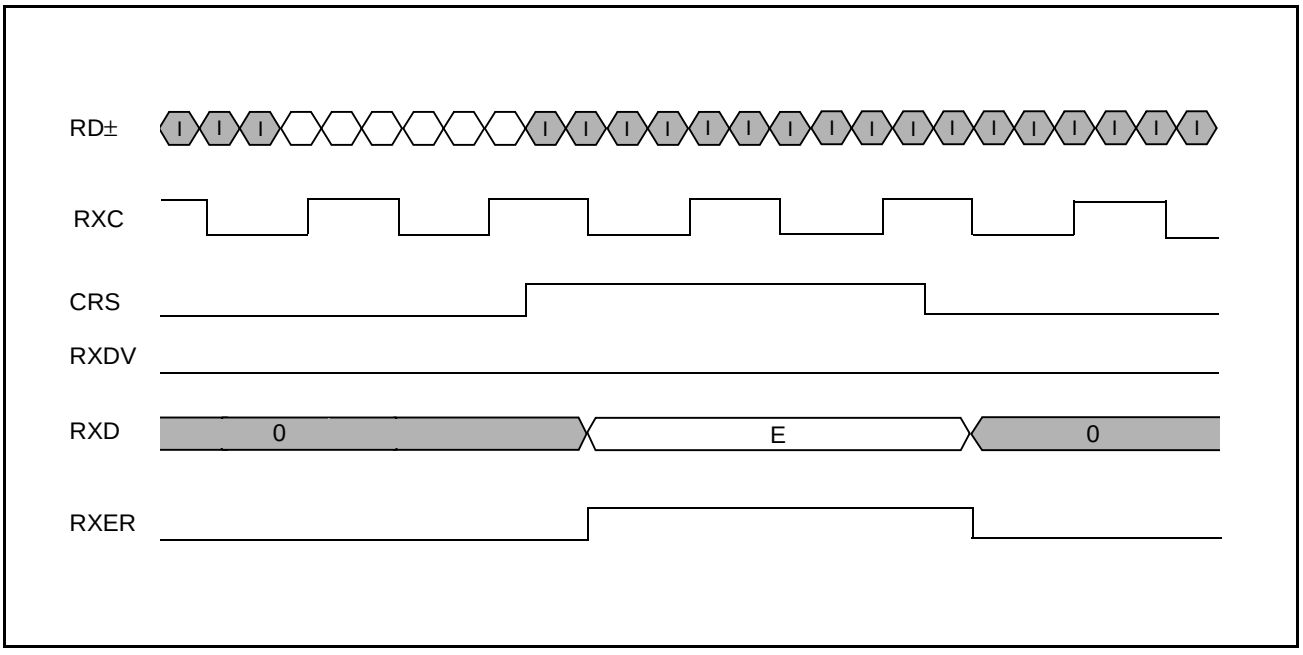


Table 33 provides the parameters for 10BASE-T transmit timing. Figure 11 illustrates 10BASE-T transmit start of timing packet.

Table 33: 10BASE-T Transmit Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
TXC Cycle Time (10BASE-T)	TXC_CYCLE	395	400	405	ns
TXC High/Low Time (10BASE-T)		197.5	200	202.5	ns
TXC Rise/Fall Time		2		5	ns
TXC Rising edge to TXEN valid	TXC_TXEN_VALID			25	ns
TXC Rising edge to TXEN hold	TXC_TXEN_HOLD	75			ns
TXC Rising edge to TXD valid	TXC_TXD_VALID			25	ns
TXC Rising edge to TXD hold	TXC_TXD_HOLD	75			ns
TD± after TXEN Assert	TXEN_TDATA	–	400	450	ns
CRS Assert after TXEN Assert	TXEN_CRS	–	50	100	ns
CRS Deassert after TXEN Deassert	TXEN_CRS_EOP	–	770	1200	ns
COL Assert after TXEN Assert (while RX)	TXEN_COL				
COL Deassert after TXEN Deassert (while RX)	TXEN_COL_EOP				
Idle on Twisted Pair after TXEN De-Assert	TX_QUIET	–	460	500	ns
Note: TXD, TXEN delivered to the BCM5201/5202 should be generated of the rising edge of TXC.					

Figure 11: 10BASE-T Transmit Start of Packet Timing

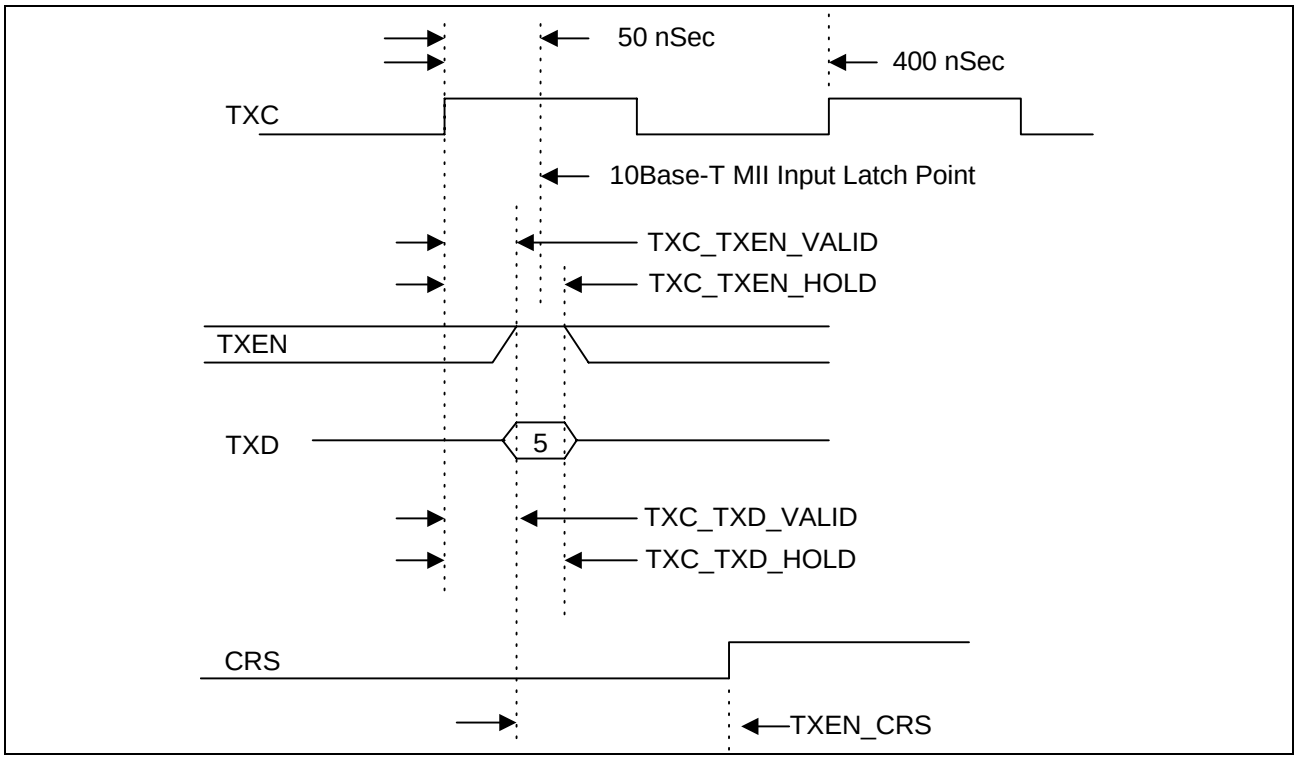


Table 34 provides the parameters for 10BASE-T receive timing. 10BASE-T collision timing is shown in Table 35.

Table 34: 10BASE-T Receive Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RXC Cycle Time	RXC_CYCLE	370.0	400	430.0	ns
RXC High/Low Time		150.5	200	240.5	ns
CRS Assert after Receive Analog Data	RX_CRS_BT	100	150	250	ns
RXC Valid after CRS Assert	RXC_VALID	–	–	2000	ns
RXDV Assert after Receive Analog Data	RX_RXDV	–	1900	2300	ns
RXDV Deassert after Receive Analog EOP ends	RX_NOT_RXDV	–	510	560	ns
CRS Deassert after Receive Analog EOP ends	RX_NOT_CRS	–	510	560	ns

Table 35: 10BASE-T Collision Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
COL Assert after Receive Analog (while transmitting)	RX_COL	–	250	300	ns
COL Deassert after TXEN Deassert (while receiving)	TXEN_NOT_COL	–	440	490	ns
COL Assert after TXEN Assert (while receiving)	TXEN_COL	–	50	100	ns
COL Deassert after Receive Analog ends (while transmitting)	RX_NOT_COL	–	400	450	ns

Table 36, Table 37, and Table 38 provide the parameters for loopback timing, auto-negotiation timing, and LED timing.

Table 36: Loopback Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
TXD to RXD Steady State Propagation Delay		–	160	–	ns

Table 37: Auto-Negotiation Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Link Test Pulse Width		–	100	–	ns
FLP Burst Interval		5.7	16	22.3	ms
Clock Pulse to Clock Pulse		111	123	139	us
Clock Pulse to Data Pulse (Data = 1)		55.5	62.5	69.5	us

Table 38: LED Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
LED On Time (XMTLED#, RCVLED#, ACTLED#)		–	80	–	ms
LED Off Time (XMTLED#, RCVLED#, ACTLED#)		–	80	–	ms

Management data interface timing parameters are described in Table 39. Figure 12 and Figure 13 illustrate two types of management interface timing.

Table 39: Management Data Interface Timing

PARAMETER	*SYMBOL*	*MIN*	*TYP*	*MAX*	*UNIT*
MDC Cycle Time		80	–	–	ns
MDC High/Low		30	–	–	ns
MDC Rise/Fall Time		–	–	10	ns
MDIO Input Setup Time to MDC rising		10	–	–	ns
MDIO Input Hold Time from MDC rising		10	–	–	ns
MDIO Output Delay from MDC rising		0	–	50	ns

Figure 12: Management Interface Timing

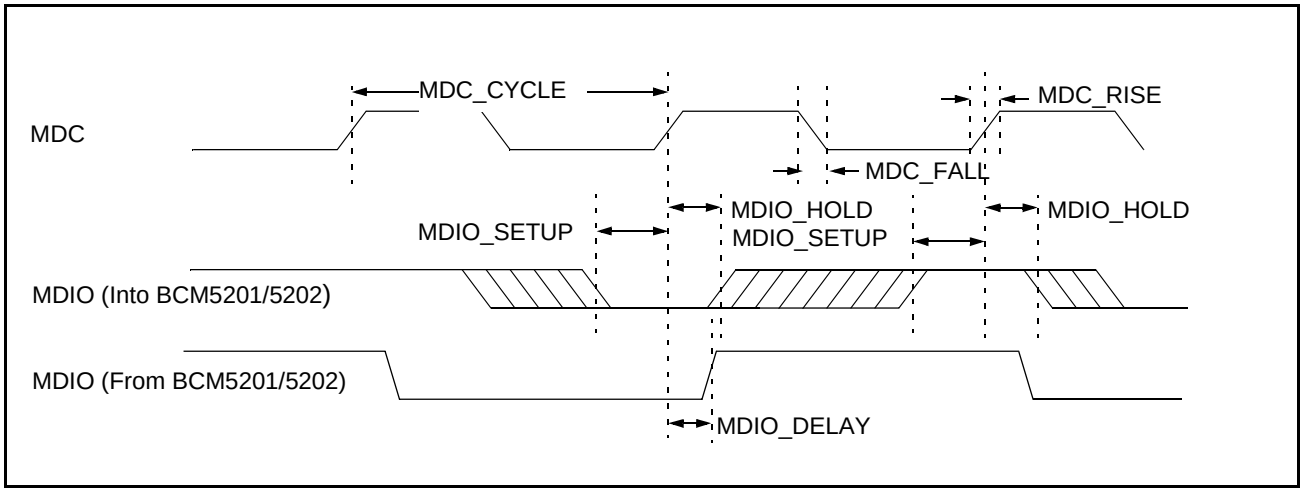
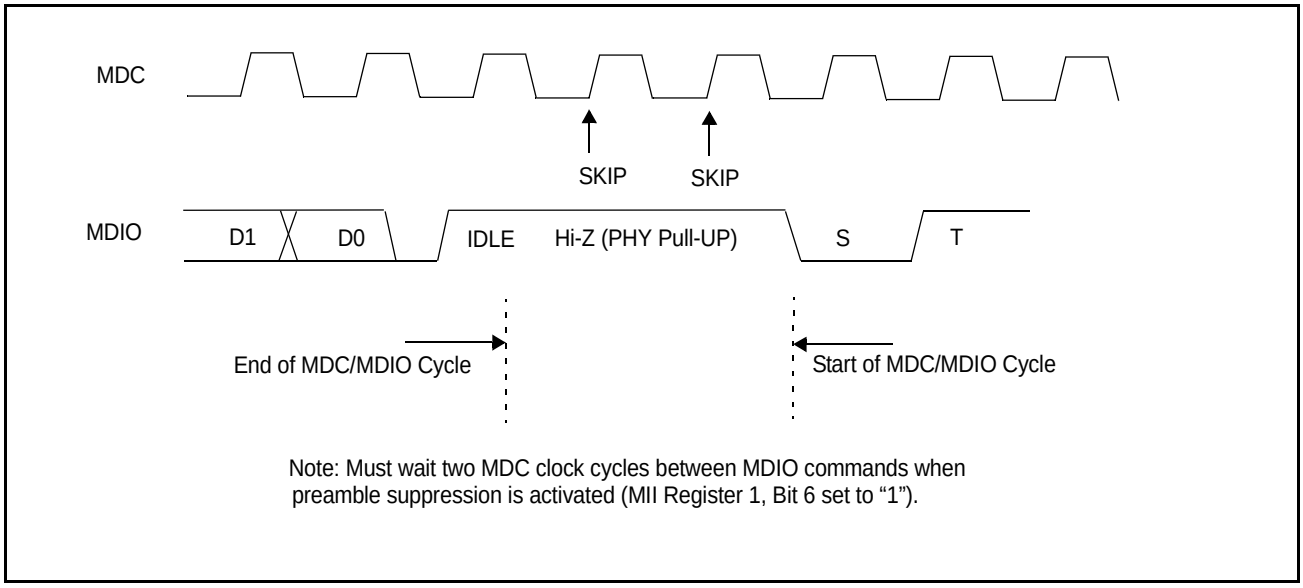


Figure 13: Management Interface Timing (with Preamble Suppression On)



Note: Must wait two MDC clock cycles between MDIO commands when preamble suppression is activated (MII Register 1, Bit 6 set to “1”).

SECTION 7: ELECTRICAL CHARACTERISTICS

Table 40 provides the absolute maximum ratings for the BCM5201 and BM5202. The recommended operating conditions for the BCM5201 and BCM5202 are shown in Table 41. Table 42 provides the package thermal characteristics. Table 43 gives the electrical characteristics of the BCM5201 and BCM5202.

Table 40: Absolute Maximum Ratings

SYMBOLS	*PARAMETERS*	*MIN*	*MAX*	*UNITS*
V_{DD}	Supply Voltage - Except REGDVDD, REGAVDD	GND - 0.3	5.0	V
V_{REG}	Supply Voltage - Only REGDVDD, REGAVDD	GND - 0.3	7.0	V
V_I	Input Voltage	GND - 0.3	IVDD + 0.3	V
I_I	Input Current		±10	mA
T_{STG}	Storage Temperature	–40	+125	°C
V_{ESD}	Electrostatic Discharge		1000	V
Note: These specifications indicate levels where permanent damage to the device may occur. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods may adversely affect long-term reliability of the device.				

Table 41: Recommended Operating Conditions for BCM5201/BCM5202

SYM	*PARAMETER*	*PIN*	*OPERATING MODE*	*MIN*	*MAX*	*UNITS*
V_{DD}	Supply Voltage BCM5201	AVDD, DVDD, OVDD		3.00	3.60	V
		IVDD		3.00	5.25	V
V_{DD}	Supply Voltage BCM5202	REGDVDD, REGAVDD		4.75	5.25	V
		IVDD		4.75	5.25	V
V_{IH}	High-Level Input Voltage	All Digital Inputs		2.0	IVDD	V
V_{IL}	Low-Level Input Voltage	All Digital Inputs			0.8	V
		SD±	100BASE-TX		0.4	V
V_{IDIFF}	Differential Input Voltage	RD±, SD±	100BASE-FX	150		mV
V_{ICM}	Common Mode Input Voltage	RD±	100BASE-TX	1.55	1.95	V
		RD±, SD±	100BASE-FX	1.55	1.95	V
T_A	Ambient Operating Temperature - 5201			0	85	°C
T_A	Ambient Operating Temperature - 5202			0	70	°C

Table 42: Package Thermal Characteristics

	THETA ja	*THETA jc*	*UNITS*
BCM5201 KPF	53.4		°C/W
BCM5202 KET	33.0	3.5	°C/W
BCM5202 KPF	39.7	3.5	°C/W
Note: Units are in degrees centigrade per watt.			

Table 43: Electrical Characteristics

SYM	PARAMETER	PINS	CONDITIONS	MIN	TYP	MAX	UNITS
I_{DD}	Supply Current	AVDD, DVDD, OVDD, IVDD	**BCM5201**				
			Auto-Negotiation		150	160	mA
			10BASE-T Idle		110	135	mA
			10BASE-T Active		195	210[1]	mA
			100BASE-TX		205	230[2]	mA
I_{DD}	Supply Current	REGAVDD REGDVDD	**BCM5202**				
			Auto-Negotiation		150	160	mA
			10BASE-T Idle		110	120	mA
			10BASE-T Active		195	210[1]	mA
			100BASE-TX		215	230[2]	mA
I_{DD}	Supply Current Low Power mode	AVDD, DVDD, OVDD, IVDD	**BCM5201**				
			LOWPWR = 1 RESET# = 1		10	12	mA
I_{DD}	Supply Current Low Power mode	REGAVDD REGDVDD	**BCM5202**				
			LOWPWR = 1 RESET# = 1		10	20	mA
I_{DD}	Supply Current Power Off mode	AVDD, DVDD, OVDD, IVDD for BCM5201 REGAVDD, REGDVDD for BCM5202	LOWPWR = 1 RESET# = 0			5	mA
V_{OH}	High-Level Output Voltage	All Digital Outputs	I_{OH} = –15 mA	2.4			V
		TD±	driving loaded magnetics module			VDD + 1.5	V
V_{OL}	Low-Level Output Voltage	All Digital Outputs	I_{OL} = 8 mA			0.4	V
		TD±	driving loaded magnetics module	VDD – 1.5			V
V_{ODIFF}	Differential Output Voltage	TD±	100BASE-FX Mode	400			mV
I_I	Input Current	Digital Inputs w/ Pull-Up Resistors	V_I = IVDD				µA
			V_I = DGND				µA
		Digital Inputs w/ Pull-Down Resistors	V_I = IVDD				µA
			V_I = DGND				µA
		All other Digital Inputs	DGND ≤ V_I ≤ IVDD			±100	µA
I_{OZ}	High-Impedance Output Current	All Three-state Outputs	DGND ≤ V_O ≤ OVDD				µA
		All Open-drain Outputs	V_O = OVDD				µA
V_{BIAS}	Bias Voltage	RDAC		1.18		1.30	V

Note 1: Of this value, 85 mA flows through the transformer and output stage.
Note 2: Of this value, 40 mA flows through the transformer and output stage.
Note 3: Current measurements are based on “nominal” process material.

SECTION 8: APPLICATION EXAMPLES

Figure 14: Power Connections

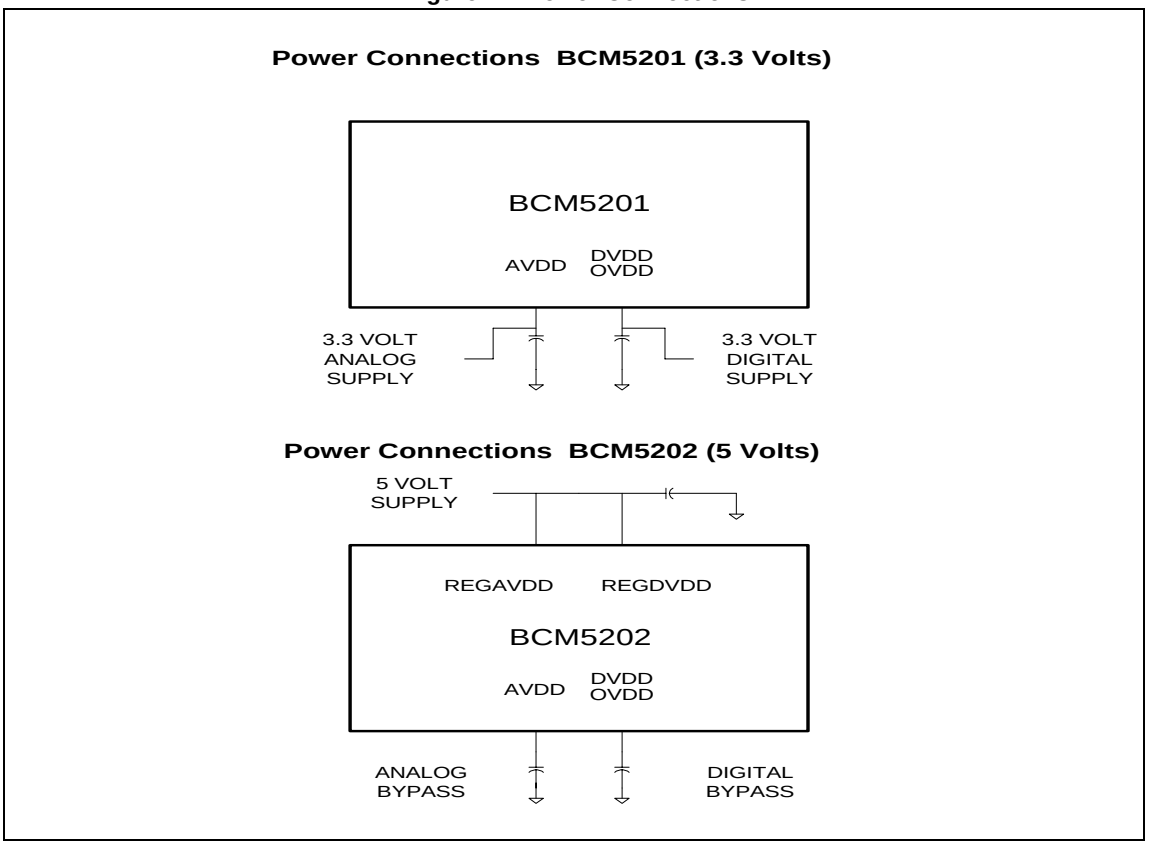
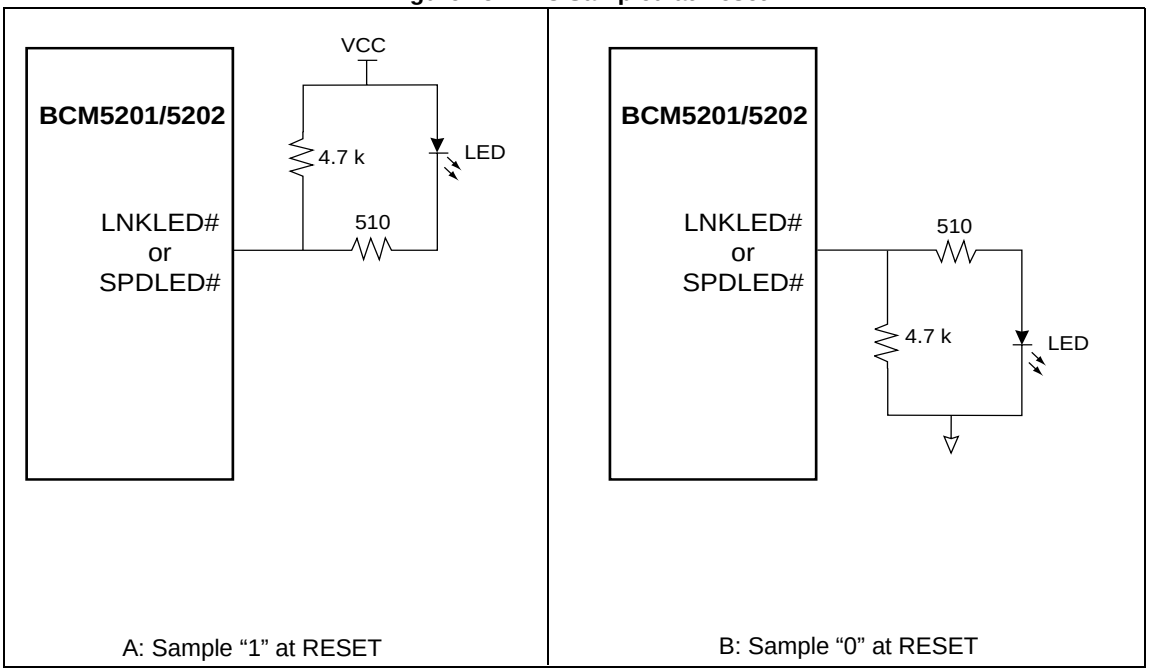
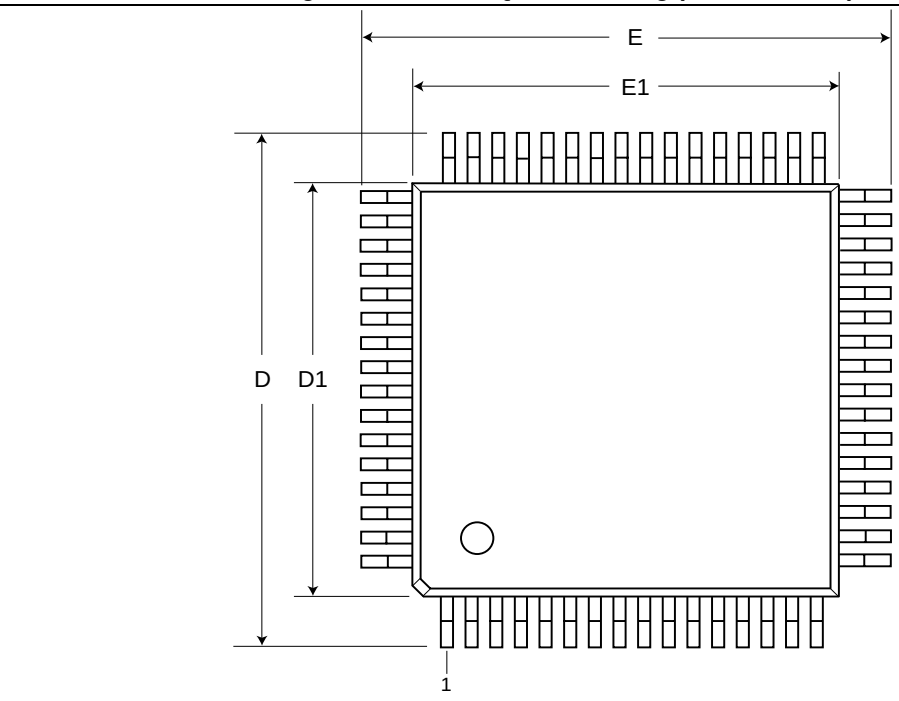


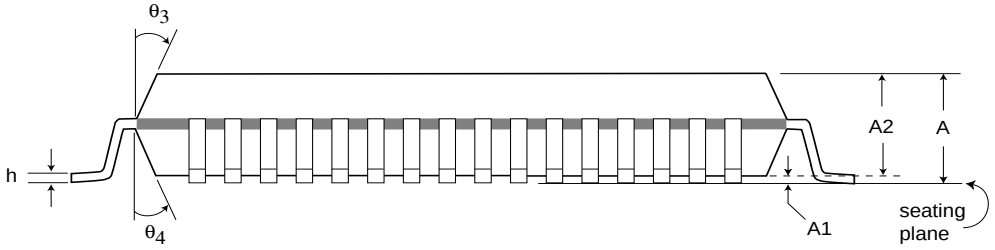
Figure 15: Pins Sampled at Reset



SECTION 9: MECHANICAL INFORMATION

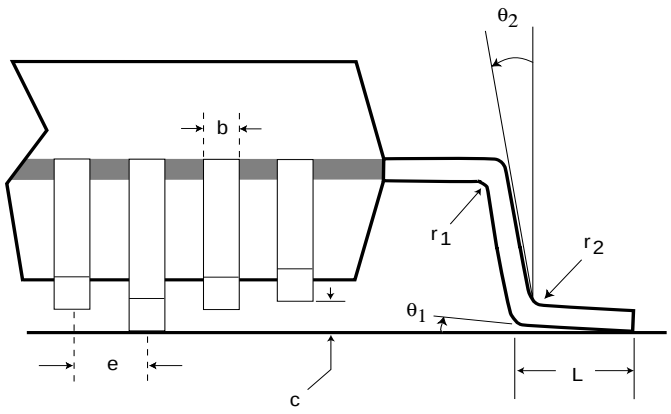
Figure 16: 64-Pin TQFP 10mm Pkg (BCM5201 KPT)





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
L	0.50	0.60	0.75
b	0.17	0.22	0.27
h	—	—	0.17
e	0.50		
c	—	—	0.08
r_1	—	0.20	—
r_2	—	0.20	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	12°	—
θ_4	—	12°	—

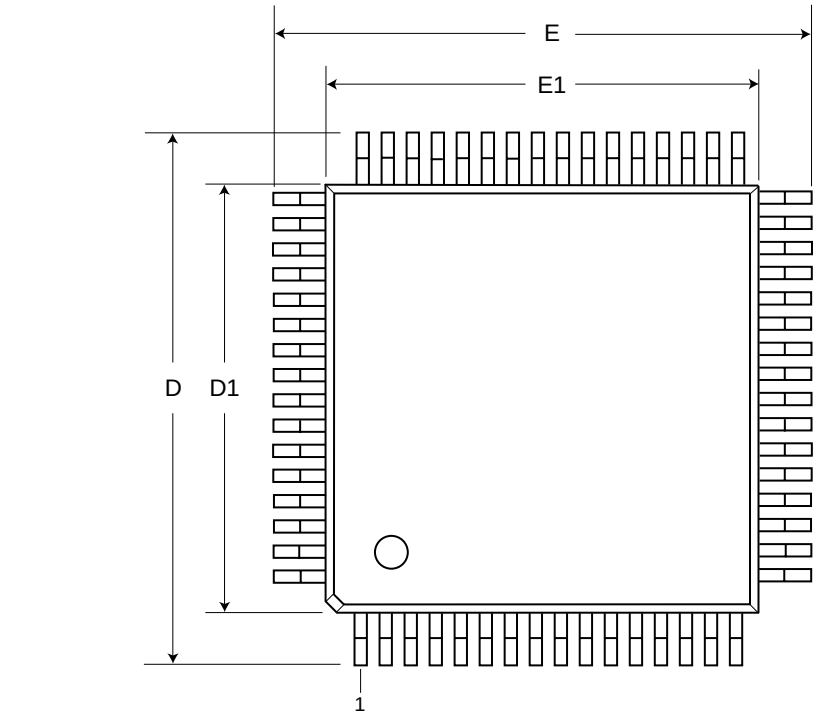
64-pin detail TQFP 10mm

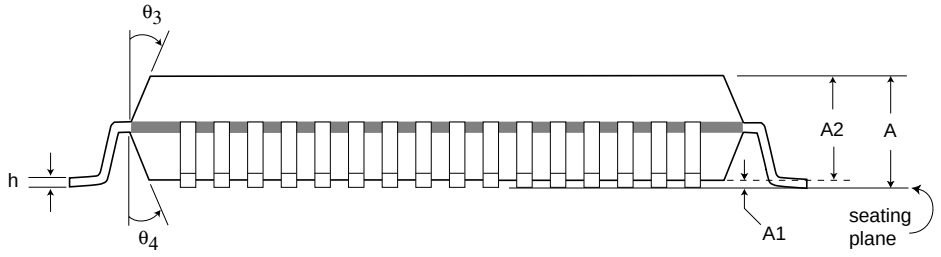


Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

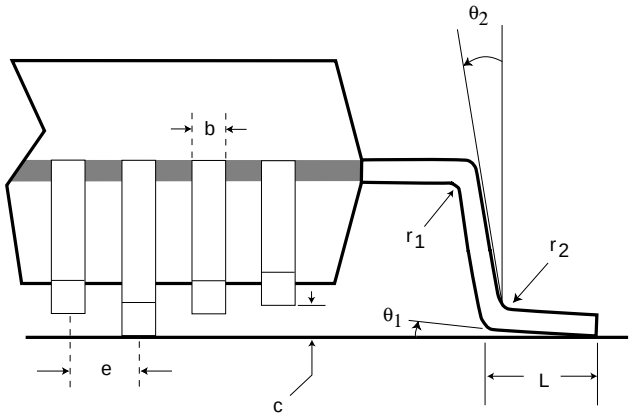
Figure 17: 64-Pin TQFP 14mm Pkg (BCM5202 KET)





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
D	15.80	16.00	16.20
D1	13.80	14.00	14.20
E	15.80	16.00	16.20
E1	13.80	14.00	14.20
L	0.50	0.60	0.75
b	0.30	0.35	0.40
h	—	—	0.17
e	0.80		
c	—	—	0.10
r_1	—	0.20	—
r_2	—	0.20	—
θ_1	0°	—	7°
θ_2	2°	6°	10°
θ_3	—	12°	—
θ_4	—	12°	—

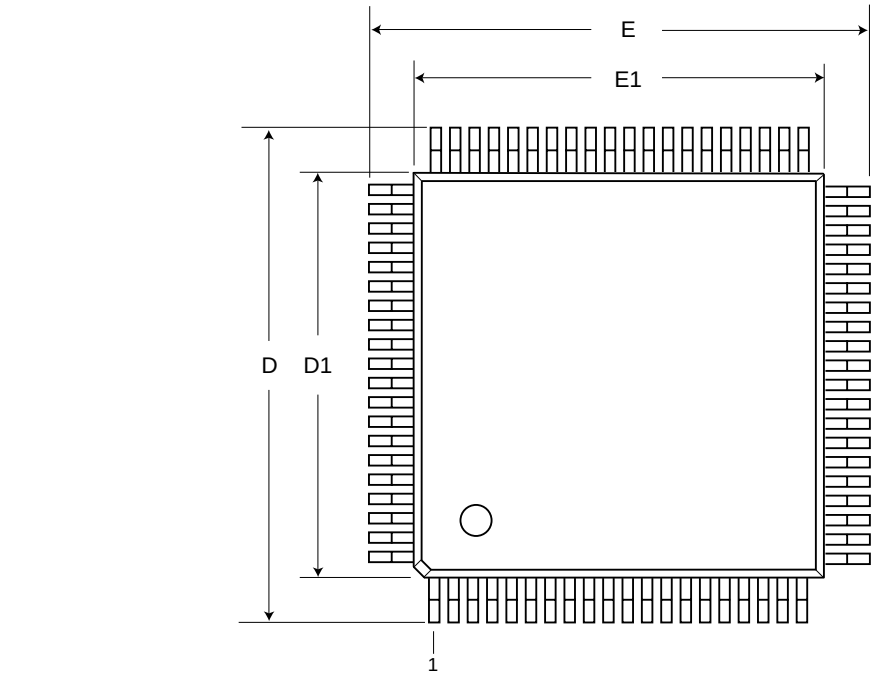
64-pin detail TQFP 14mm

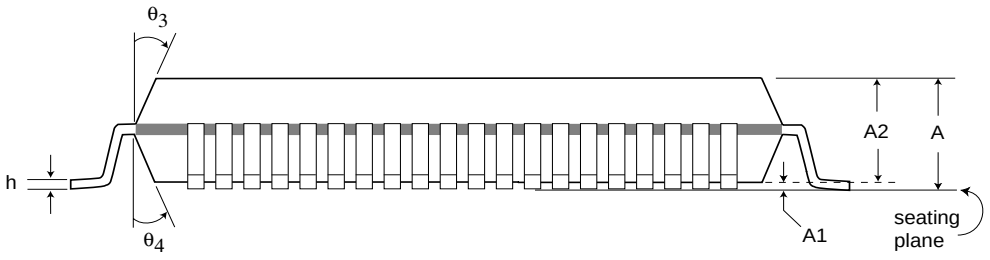


Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

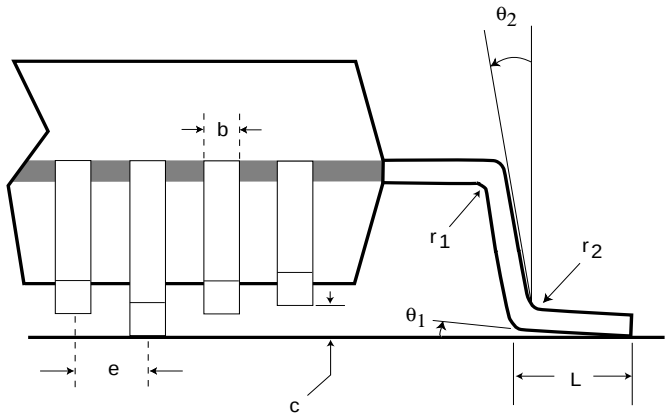
Figure 18: 80-Pin MQFP 14mm Pkg (BCM5202 KPF)





Symbol	Millimeter		
	Min	Nom	Max
A	—	—	2.45
A1	—	—	0.25
A2	1.90	—	2.10
D	16.95	—	17.45
D1	13.90	—	14.10
E	16.95	—	17.45
E1	13.90	—	14.10
L	0.73	—	1.03
b	0.22	—	0.38
h	0.13	—	0.23
e	0.65		
c	—	—	0.13
r_1	0.13	—	—
r_2	0.13	—	0.30
θ_1	0°	—	7°
θ_2	0°	—	—
θ_3	—	15°	—
θ_4	—	15°	—

80-pin detail MQFP 14mm



Notes:

1. Drawings on this page are not to scale
2. All dimensions are in millimeters except where noted
3. Foot length "L" is measured at gage plane, 0.25mm above the seating plane
4. Seating plane is defined by three lowest lead tips

SECTION 10: ORDERING INFORMATION

PART NUMBER	*PACKAGE*	*AMBIENT TEMPERATURE*
BCM5201 KPT	64-TQFP 10mm Pkg	0° to 85° C 32° to 185° F
BCM5202 KET	64-TQFP 14mm Pkg	0° to 70° C 32° to 158° F
BCM5202 KPF	80-MQFP 14mm Pkg	0° to 70° C 32° to 158° F

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